



SEAN HEELAN

**THE (IN)COMPLETE GUIDE TO
CODE ANALYSIS CARPENTRY**

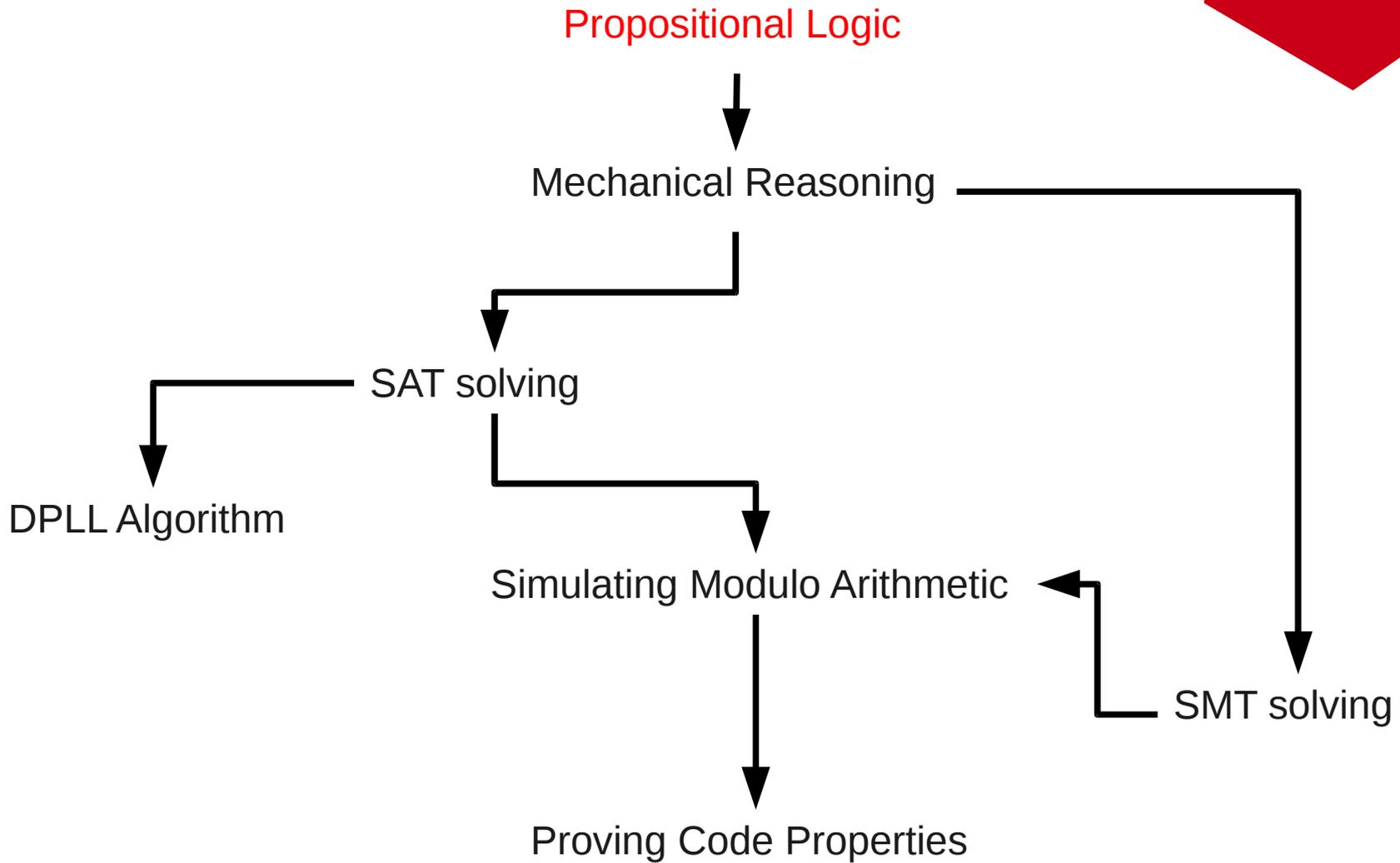
*Or how to avoid braining yourself when handed an
SMT solving hammer*

IMMUNITY INC.



```
void* ArrayBuffer::tryAllocate(unsigned numElements,
                               unsigned elementByteSize)
{
    void* result;
    // Do not allow 32-bit overflow of the total size
    if (numElements) {
        unsigned totalSize = numElements * elementByteSize;
        if (totalSize / numElements != elementByteSize)
            return 0;
    }
    if (WTF::tryFastCalloc(numElements,
                          elementByteSize).getValue(result))
        return result;
    return 0;
}
```

PART I: DOWN THE RABBIT HOLE

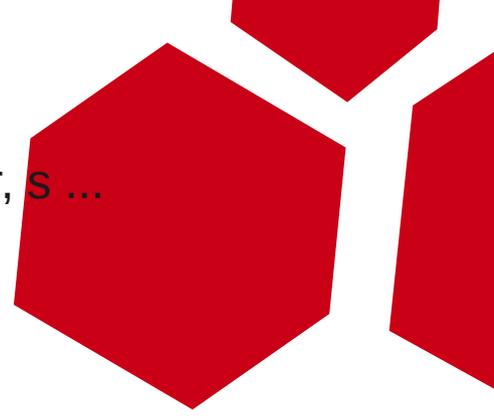


PROPOSITIONAL LOGIC



Propositional variables

$p, q, r, s \dots$



PROPOSITIONAL LOGIC

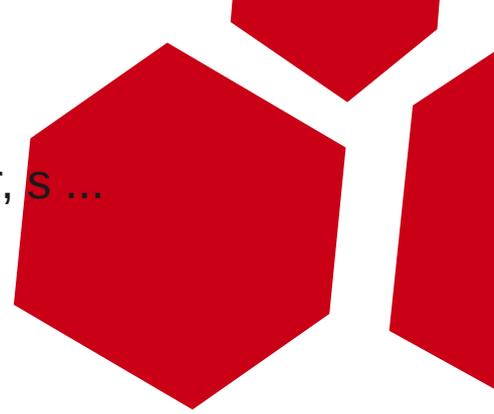


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Punctuation

$(,)$



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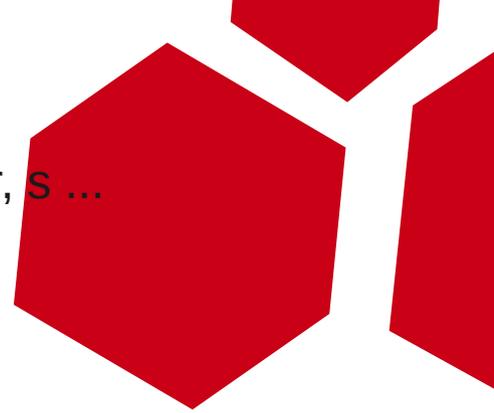
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Logical connectives

$\wedge, \vee, \sim, \rightarrow$



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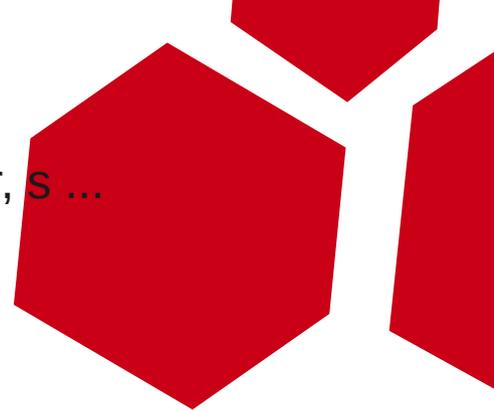
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Logical connectives

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Formation rules
(grammar)

$\sim(a \wedge b) \rightarrow c, b \sim c$



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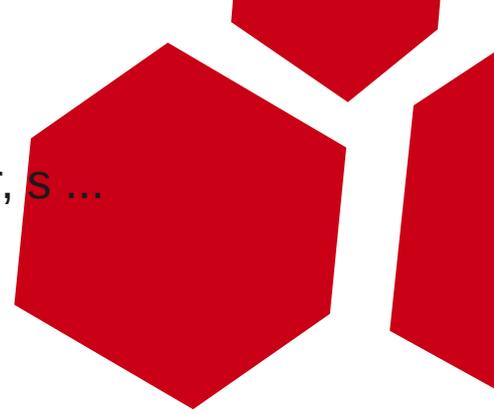
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Truth Functional

“True”/“False”



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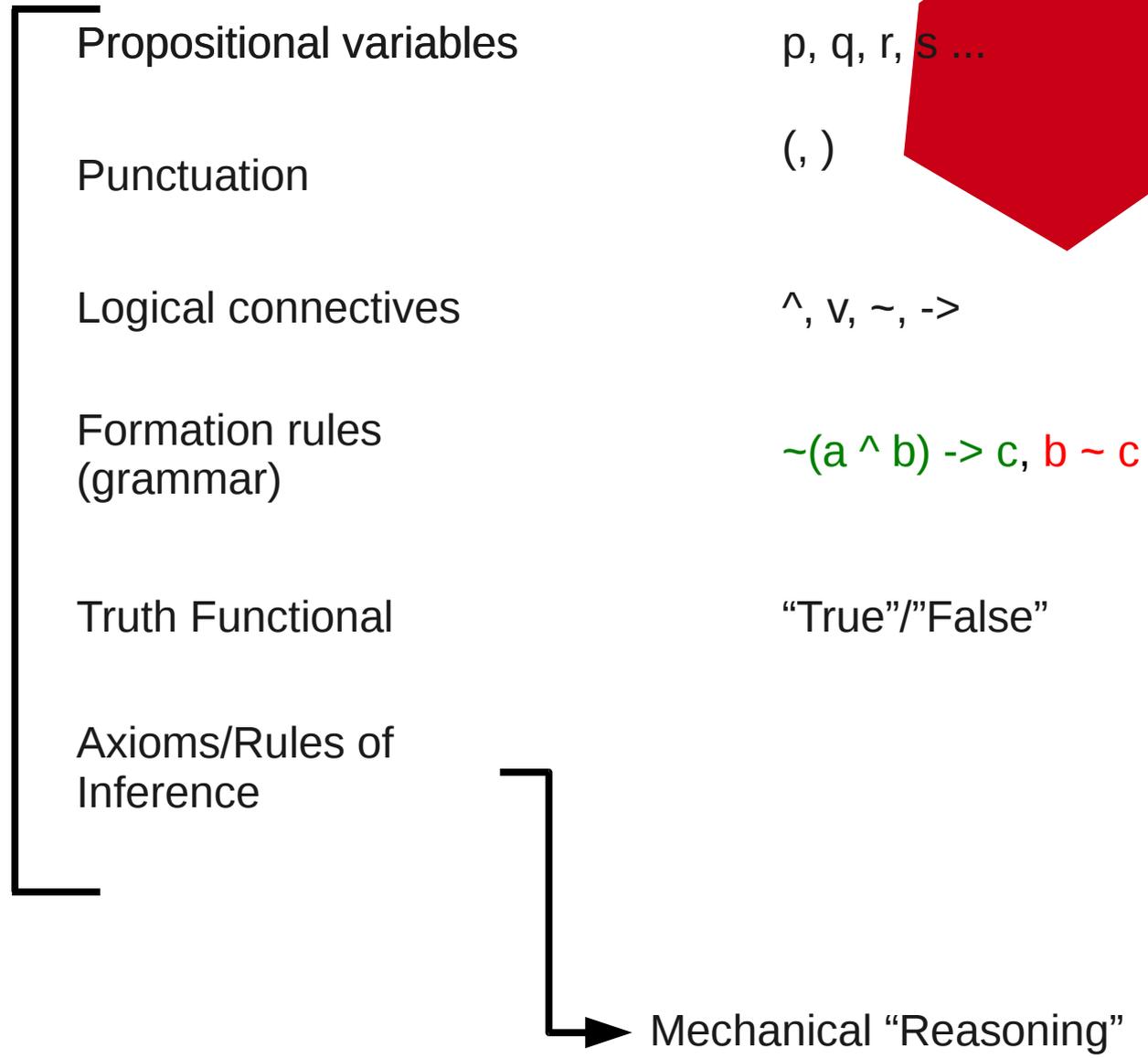
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Truth Functional

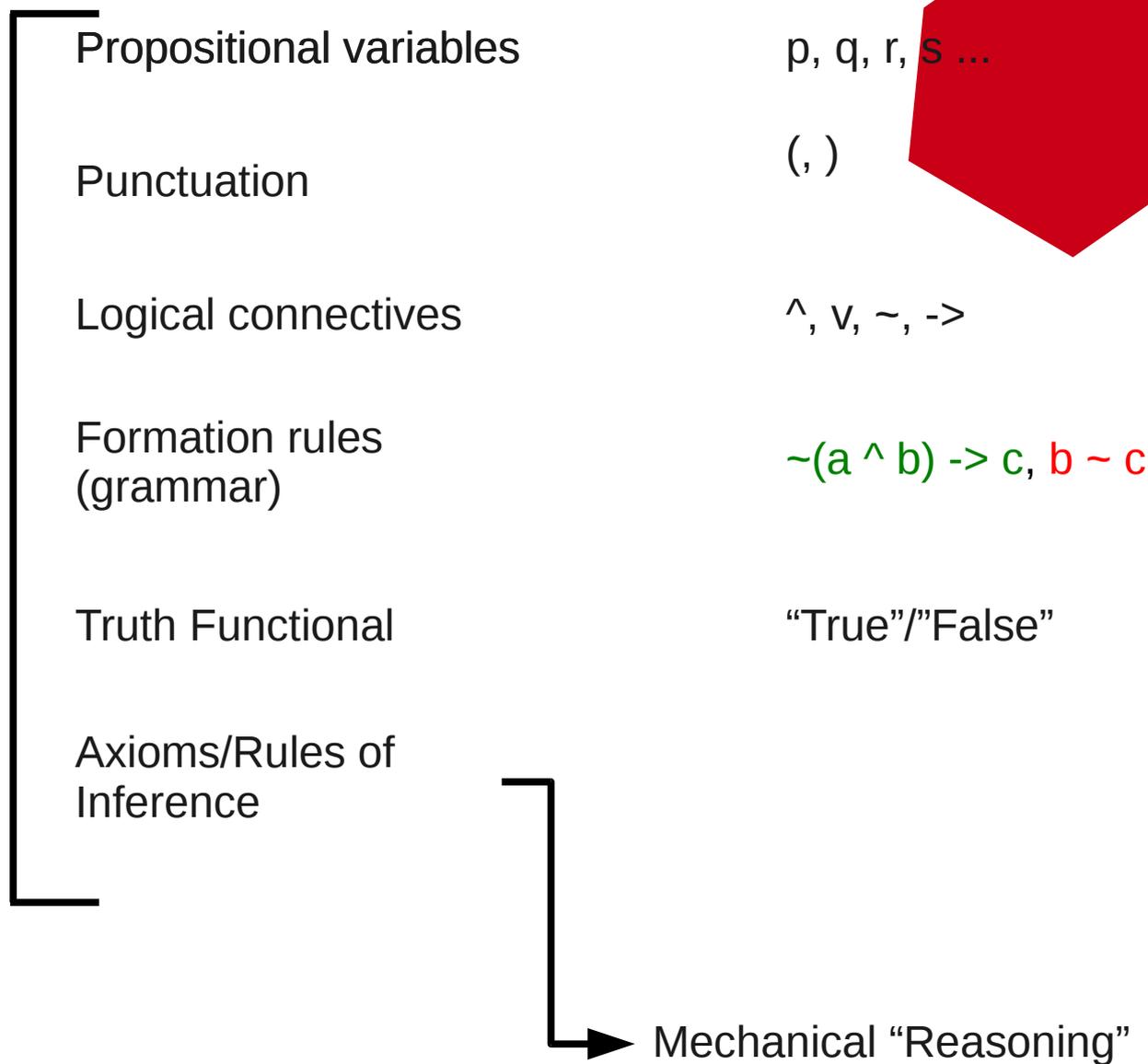
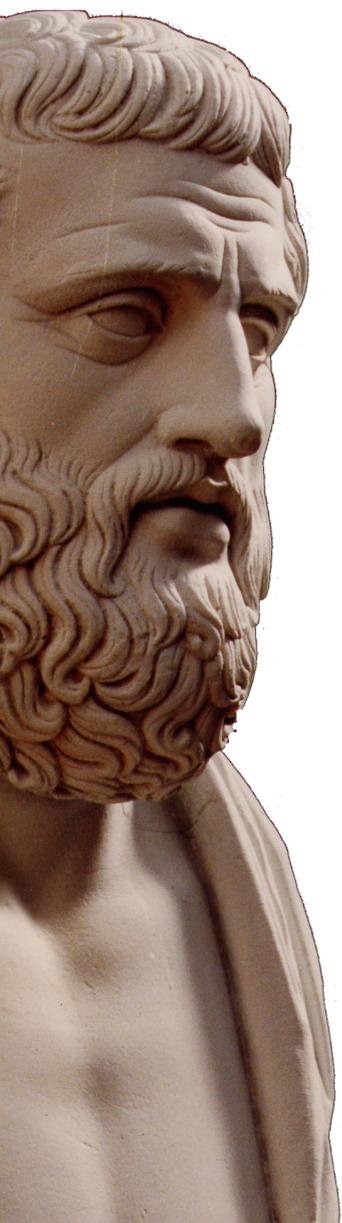
“True”/“False”

Axioms/Rules of
Inference

PROPOSITIONAL LOGIC

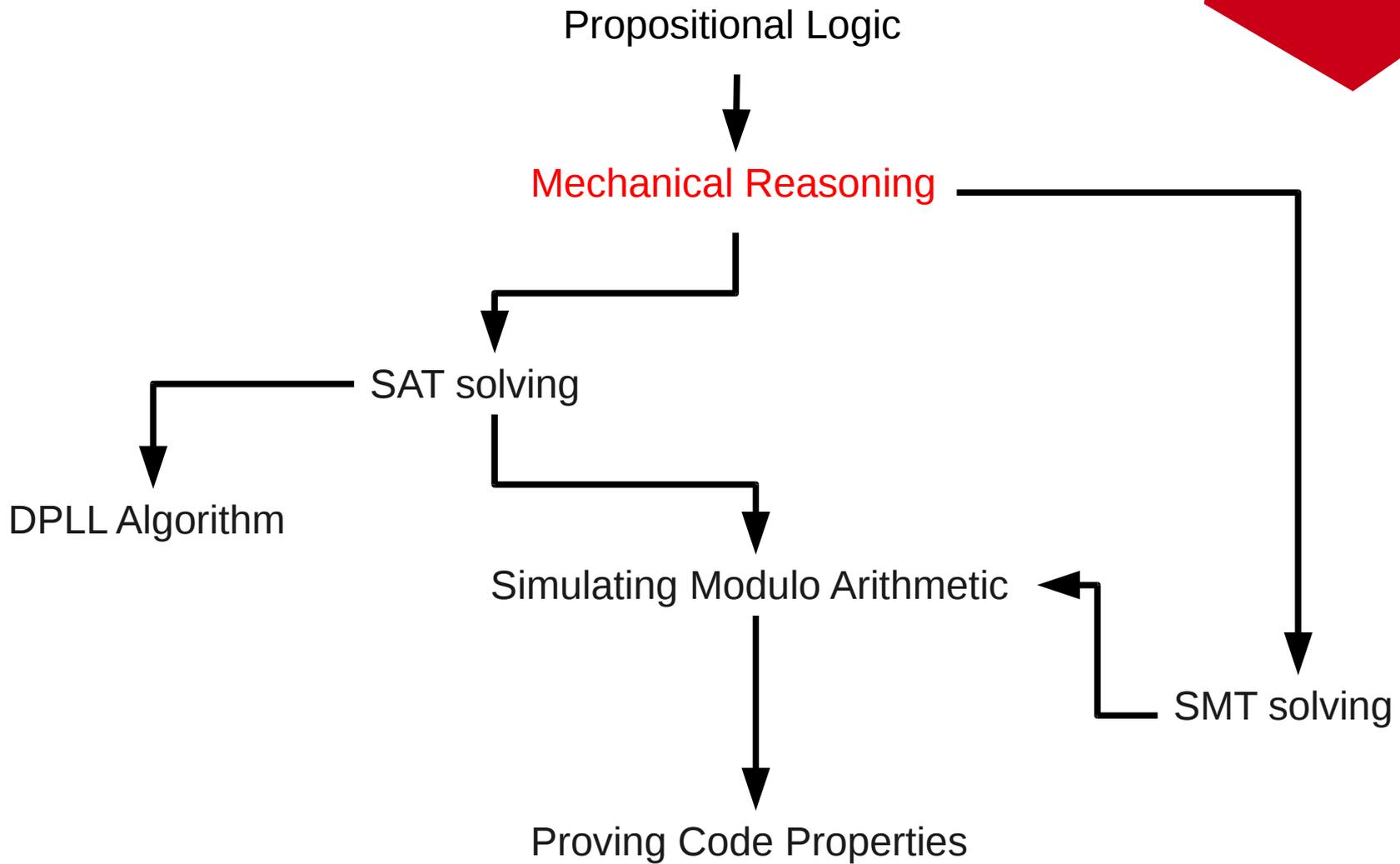


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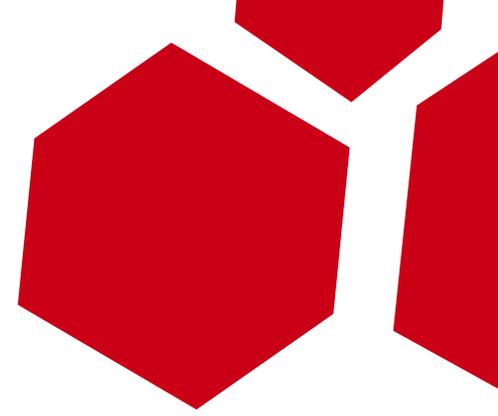
[1] This is incomplete but sufficient for our purposes. Wikipedia does a relatively good job for a lot of what we'll cover. Otherwise see <http://www.unprotectedhex.com/psv/> for books.

PART I: DOWN THE RABBIT HOLE



MECHANICAL REASONING

Truth functional \rightarrow the values for propositional variables selected from the boolean domain T/F.



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p	f^1	f^2	f^3	f^4
T	T	T	F	F
F	T	F	T	F



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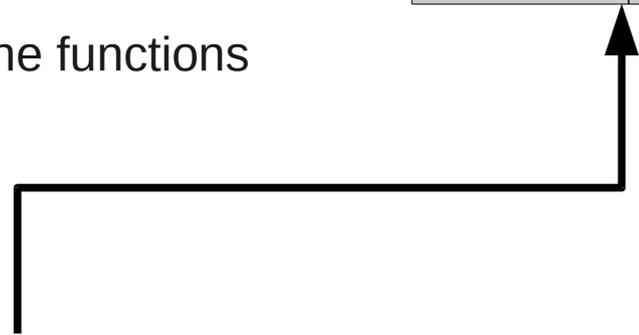
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(Truth Table)

p	$\sim p$
T	F
F	T



p	f^1	f^2	f^3	f^4
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MECHANICAL REASONING (CONT)

A 'rewriting' system for any
arbitrary propositional formula



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Evaluate $X:((a \vee b) \rightarrow (a \wedge b))$
under $a=T, b=F$



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$(a \vee b) \rightarrow (a \wedge b)$



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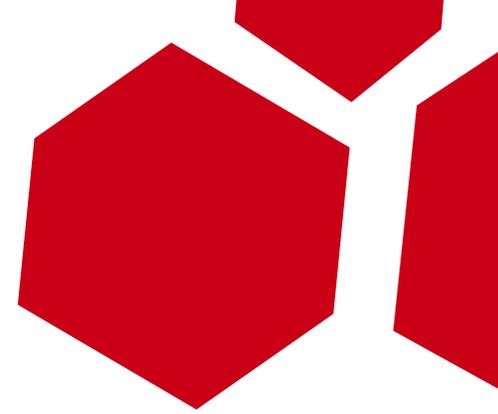
Evaluate $X:((a \vee b) \rightarrow (a \wedge b))$
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X is satisfied if it reduces to T
under any model

X is valid if it reduces to T under
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$a=T, b=F$

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Boolean satisfiability problem – *Find such an assignment
or prove that none exists*

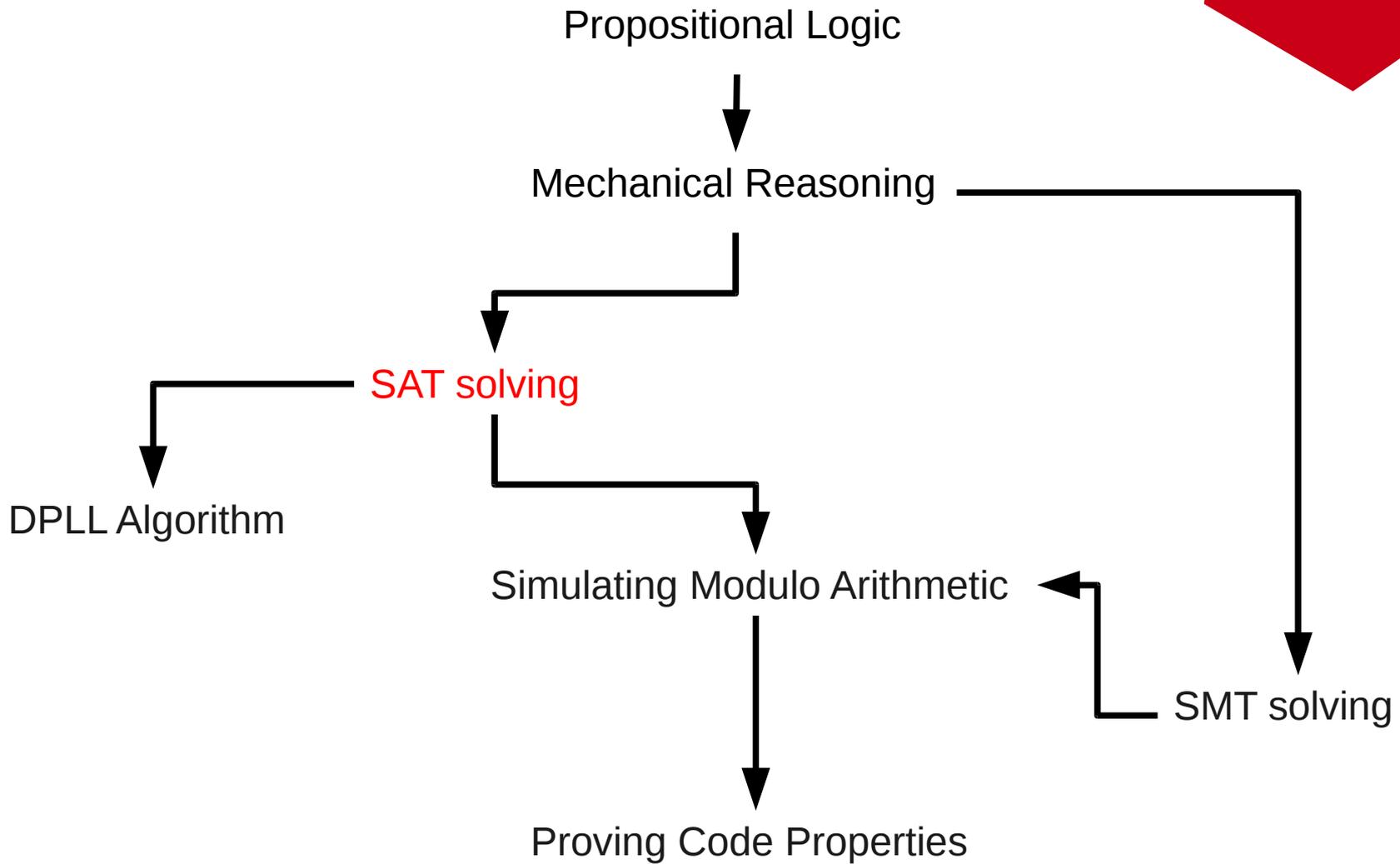
→ SAT solving

$a=T, b=F$

$(a \vee b) \rightarrow (a \wedge b)$
 $(T \vee F) \rightarrow (T \wedge F)$
 $T \rightarrow F$
 F



PART I: DOWN THE RABBIT HOLE



SAT SOLVING

SAT is a decidable problem



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The solution set is recursive
(algorithm that terminates in
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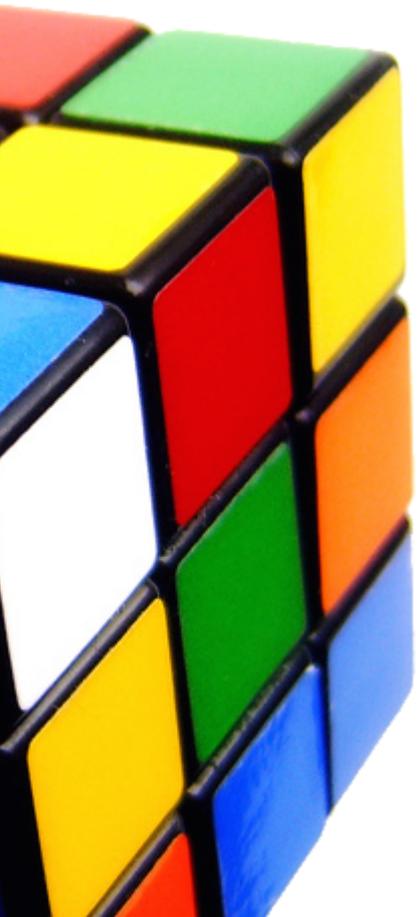
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Quite obviously won't scale, table size of 2^n but demonstrates
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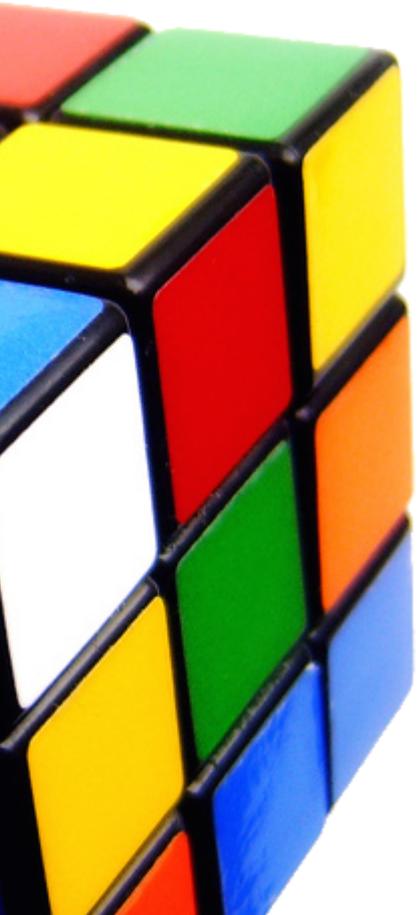


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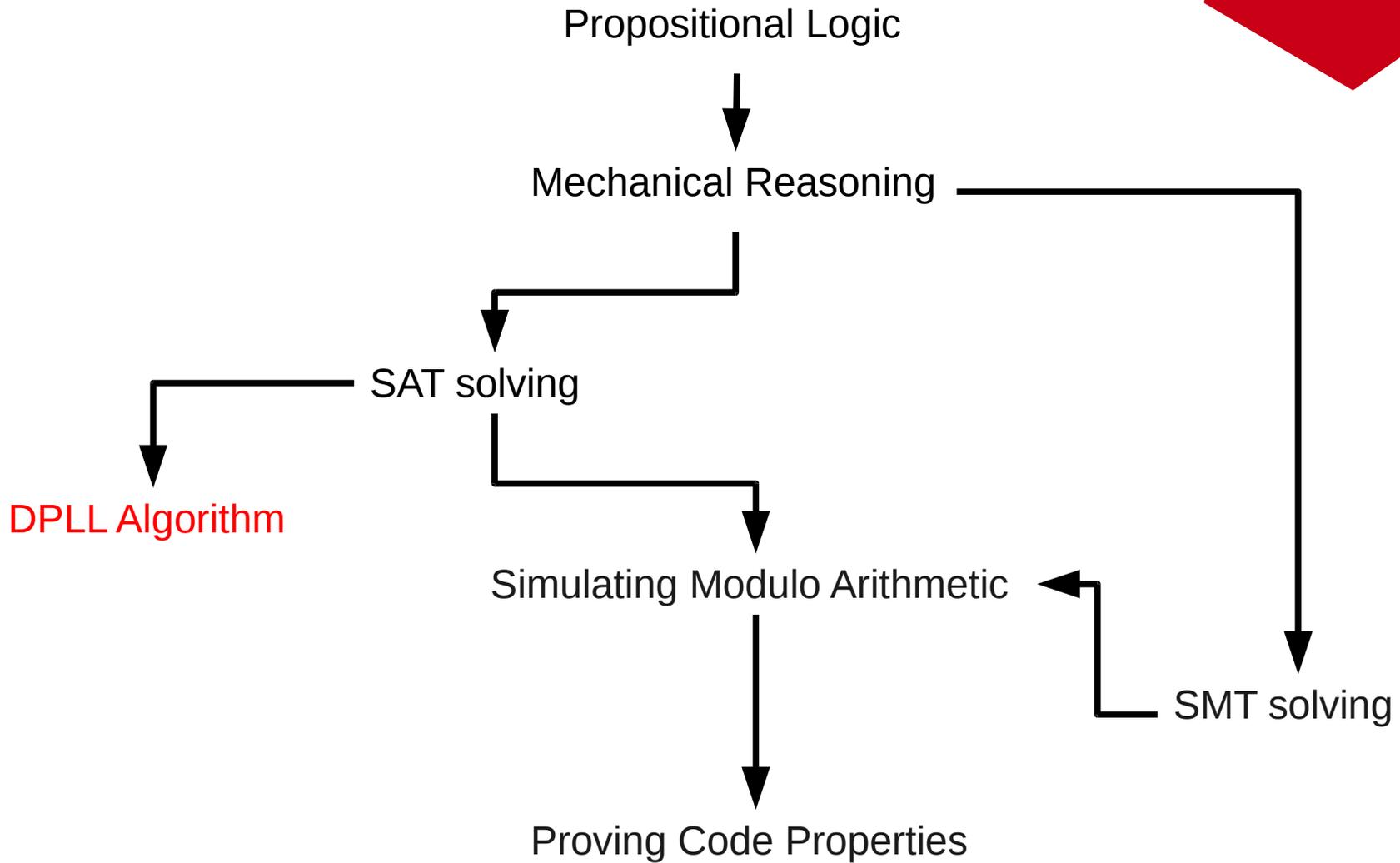
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→ DPLL Algorithm



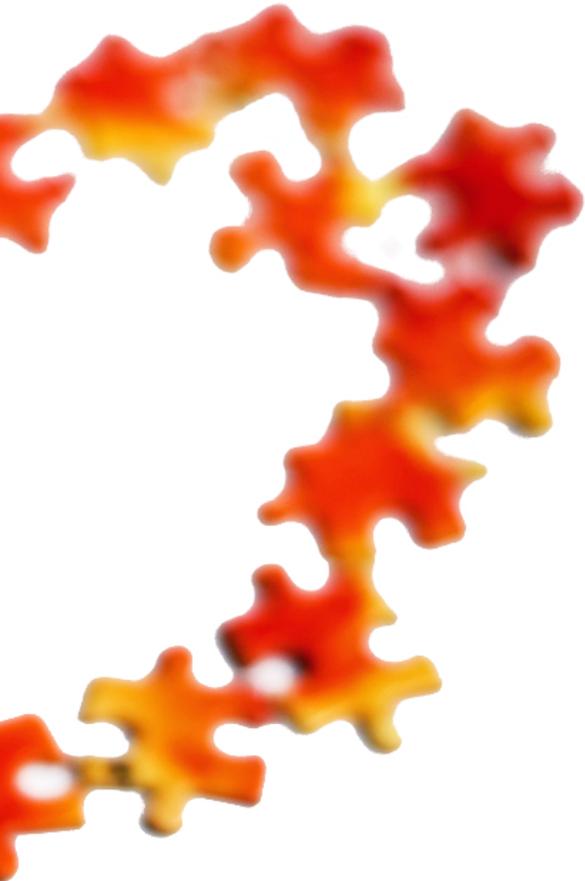
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SAT is in the NP-Complete complexity class so our worst case is always going to be exponential in the size of our input.

DPLL Algorithm – The basis for modern SAT solvers

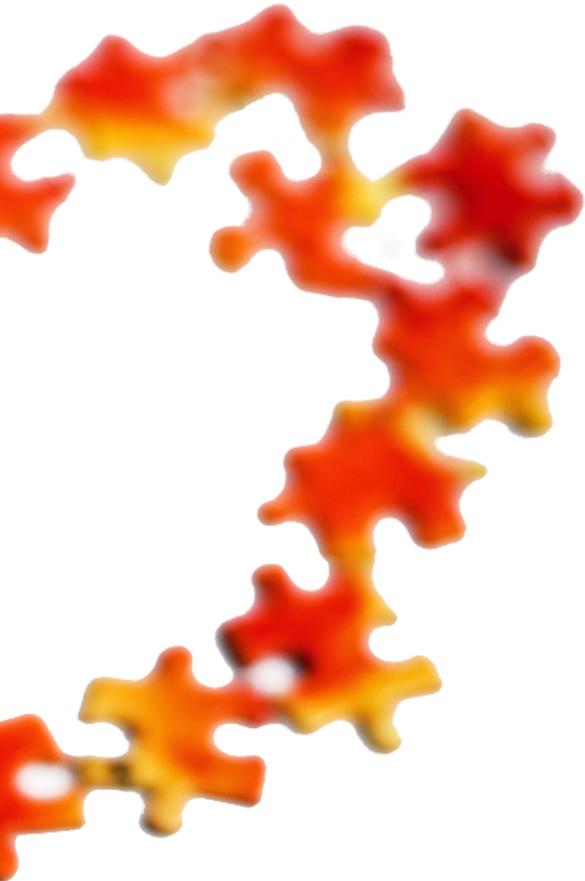


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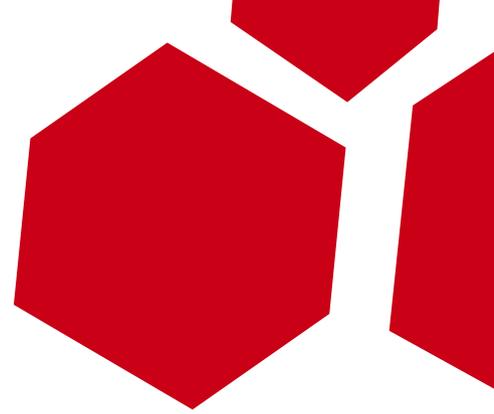
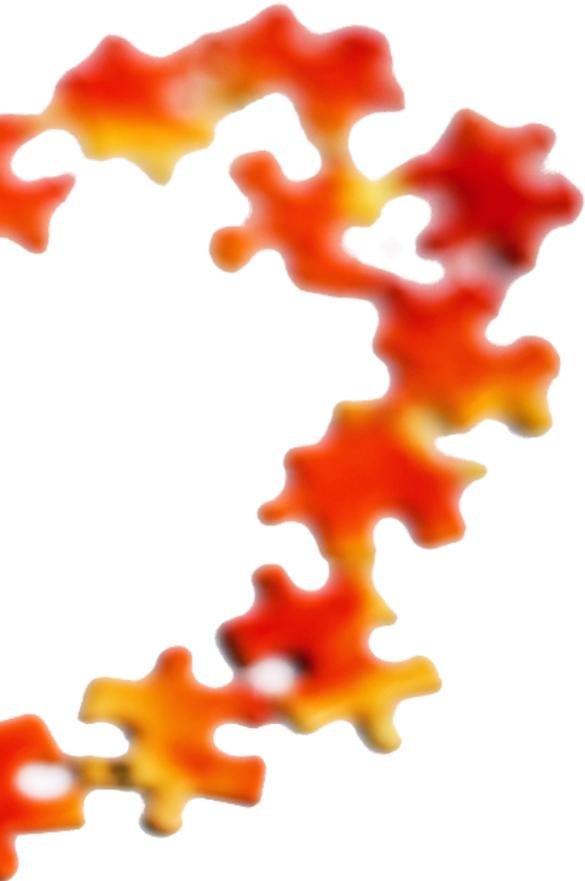


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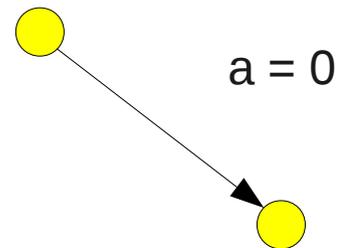


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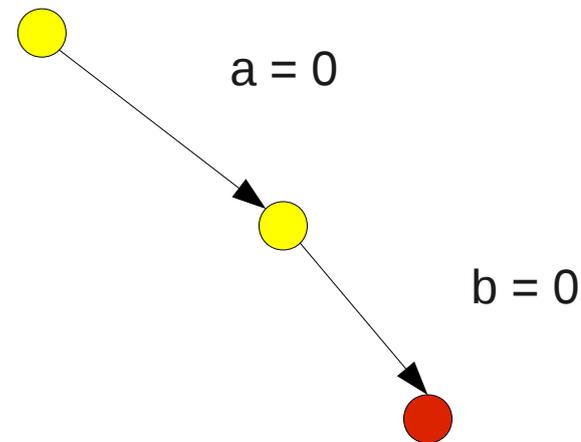


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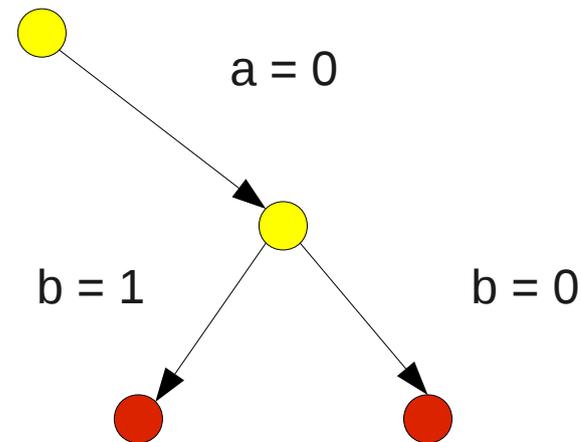


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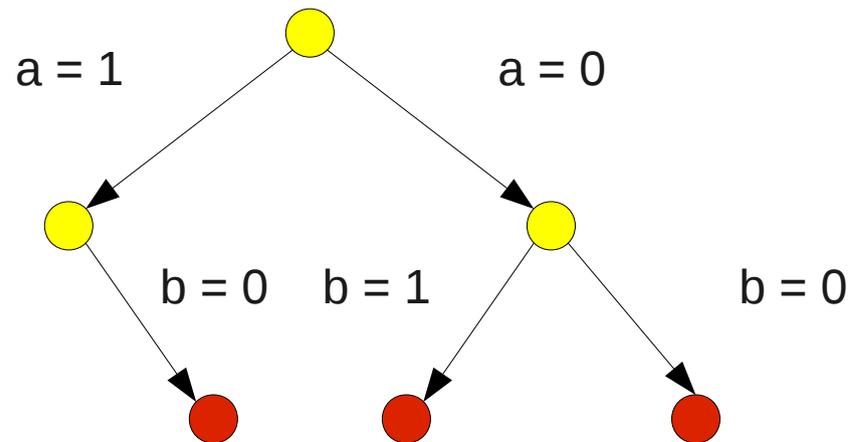


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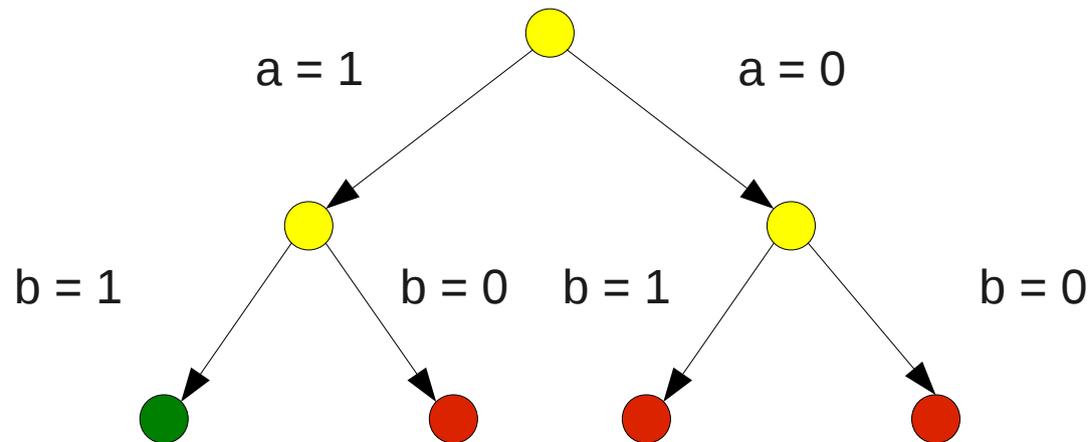


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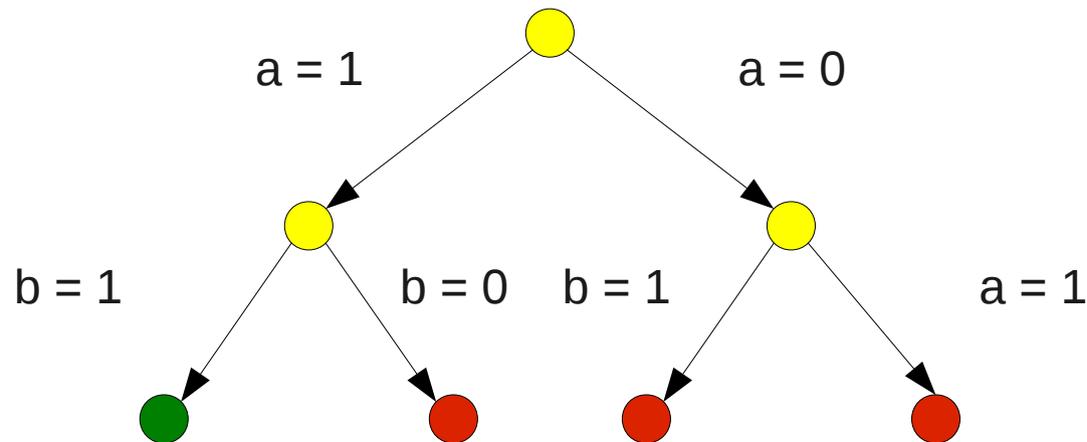


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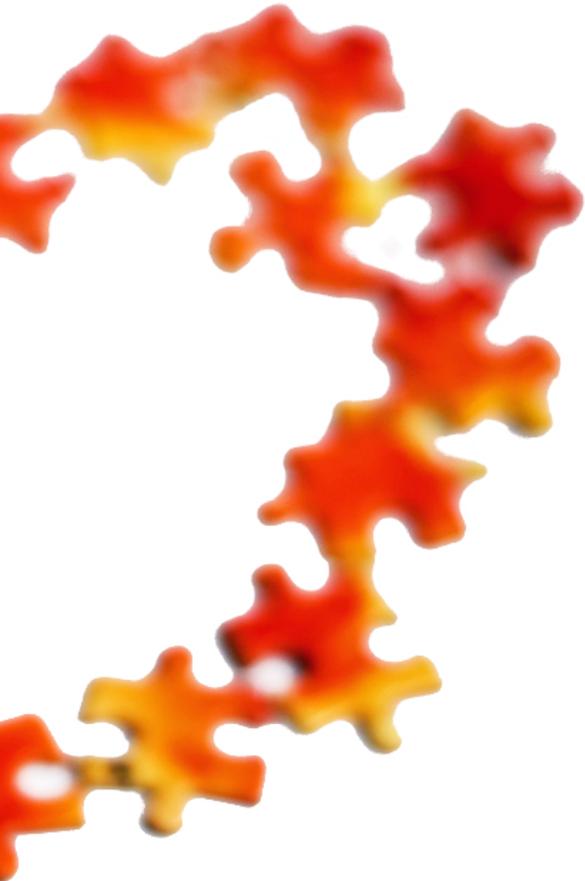
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DPLL and other optimisations work by attempting to prune the tree and limit the cases we need to consider

DPLL ALGORITHM (CONT)

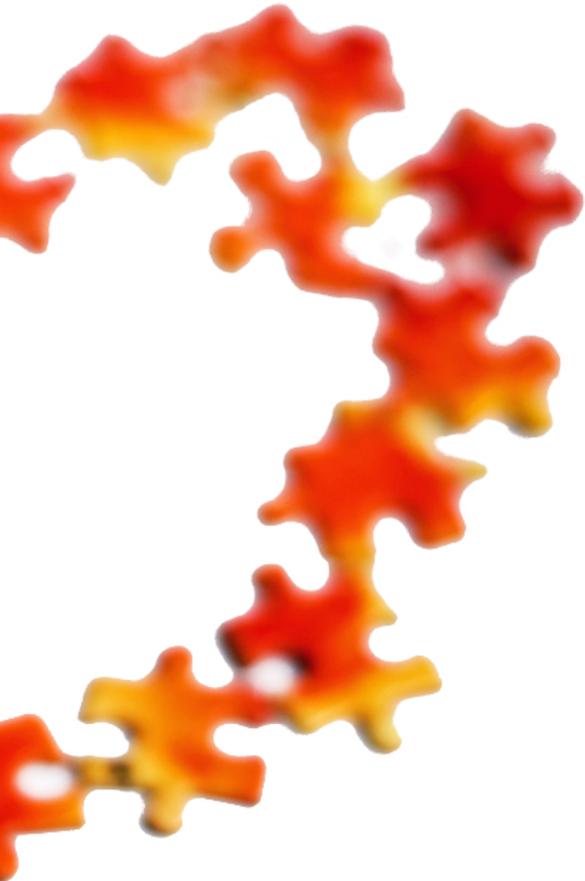
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DPLL ALGORITHM (CONT)

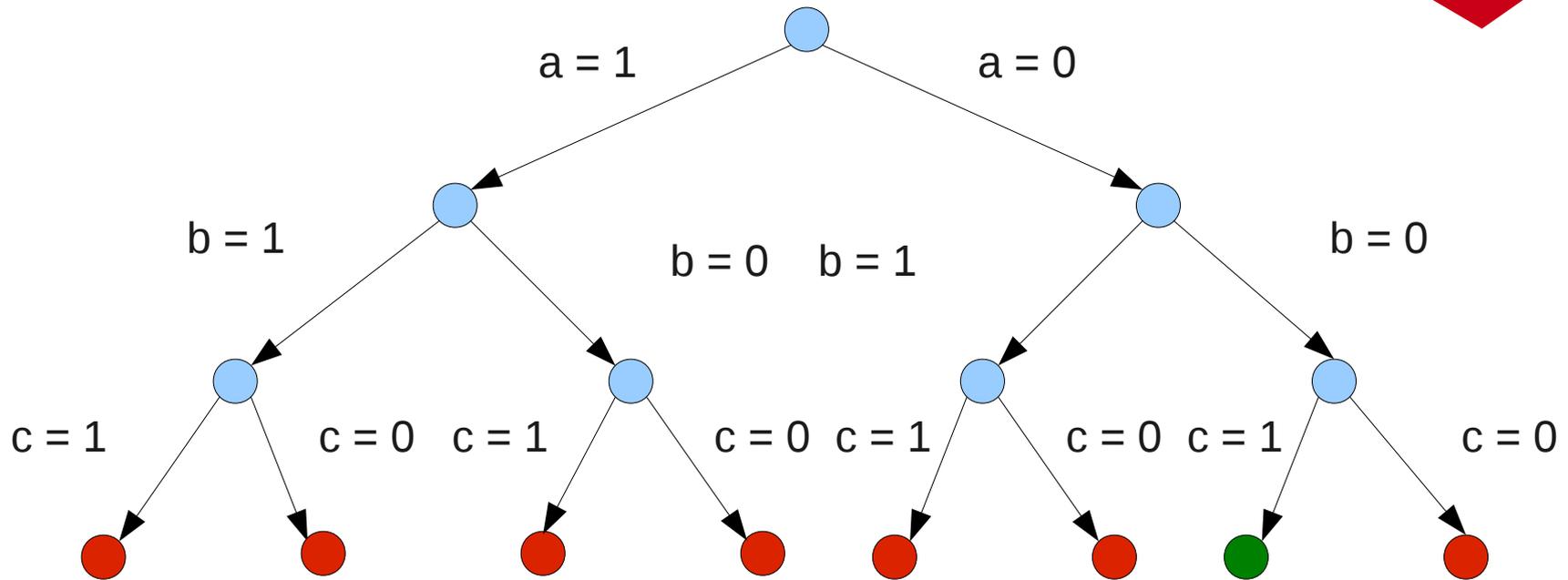
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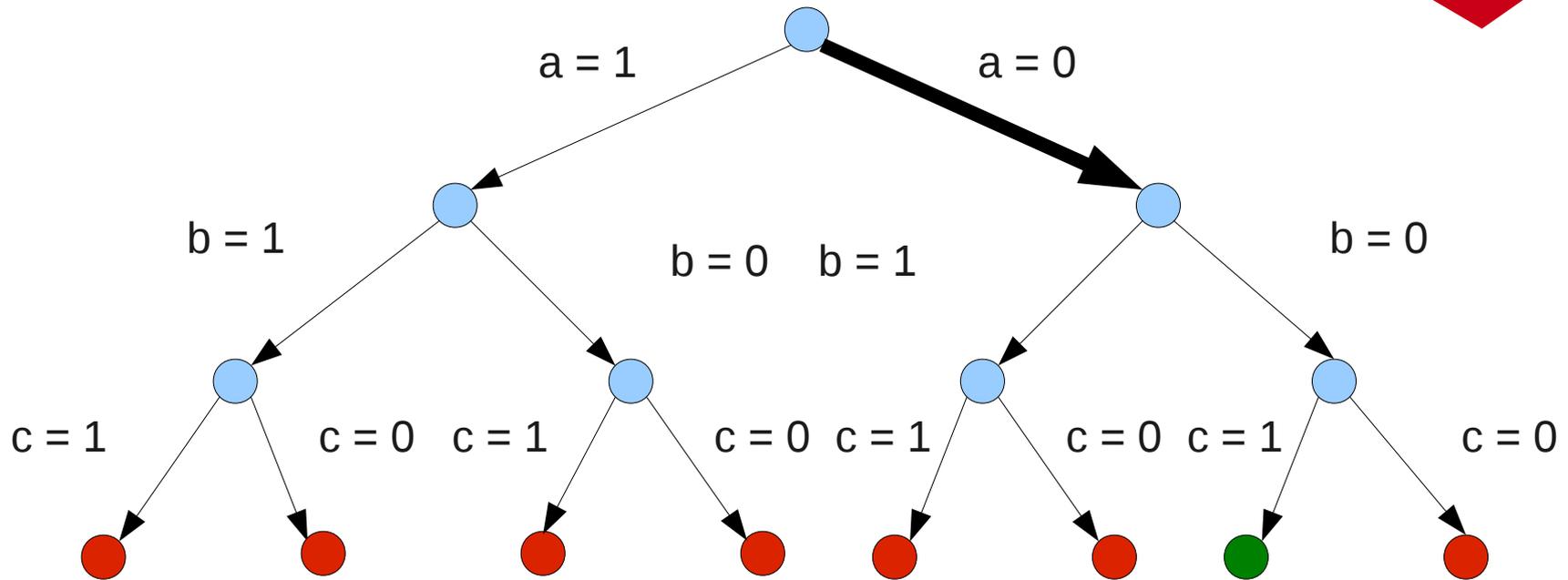
DPLL ALGORITHM (CONT)

Unit clause deduction on $(\sim a) \vee (\sim b) \vee (a \vee b \vee c)$



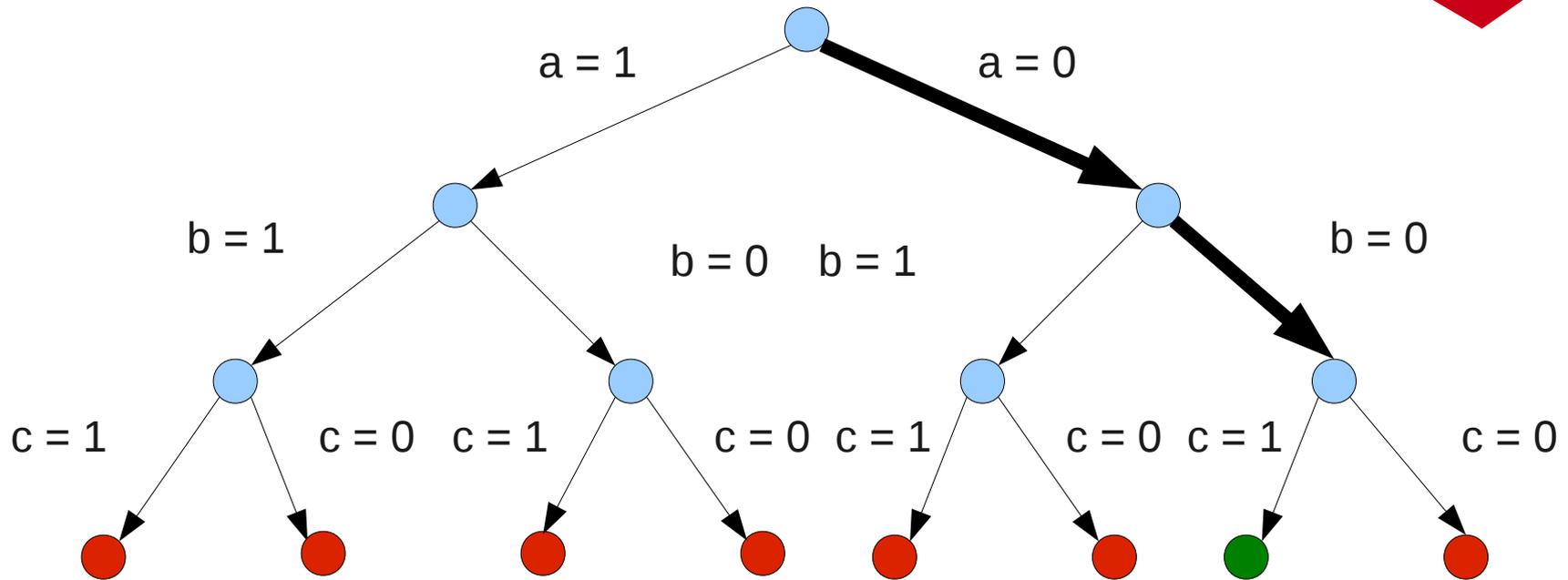
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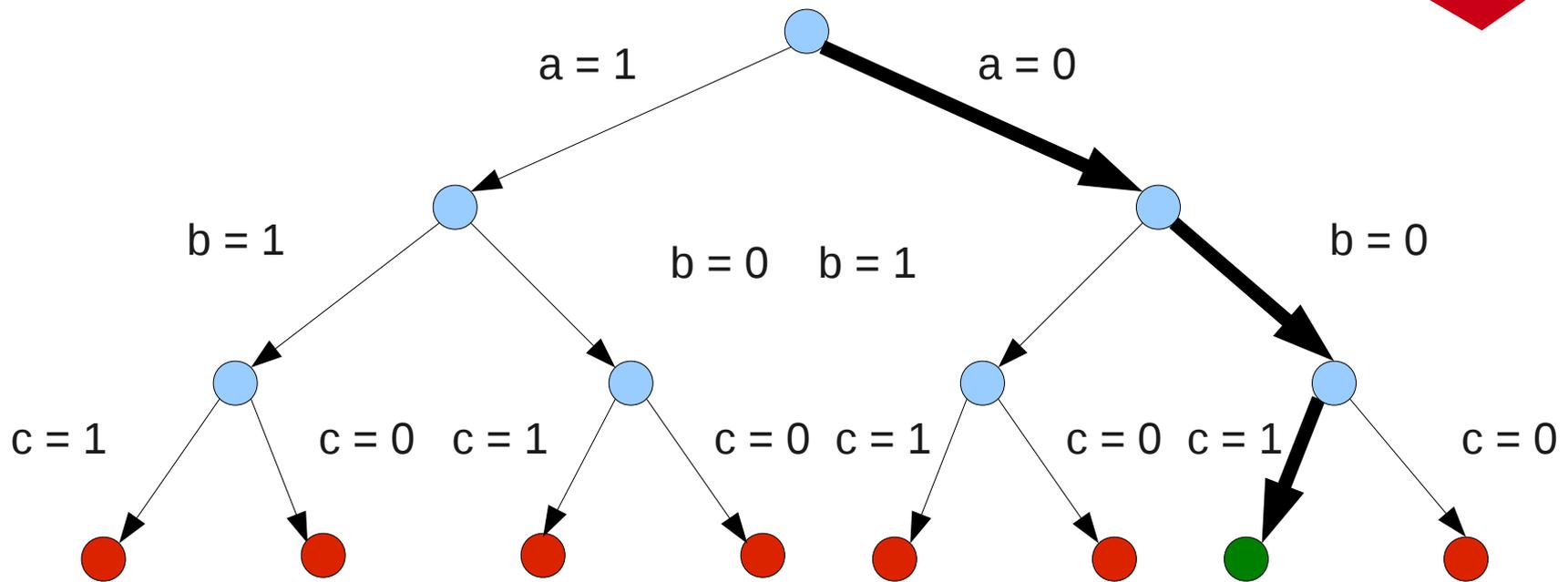
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Unit clause deduction on $(\sim a) \vee (\sim b) \vee (a \vee b \vee c)$



No search required in this case

DPLL ALGORITHM (CONT)

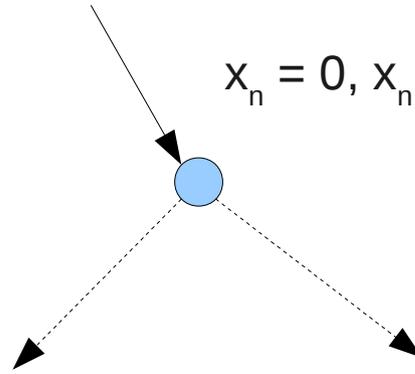
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DPLL ALGORITHM (CONT)

Clause Learning

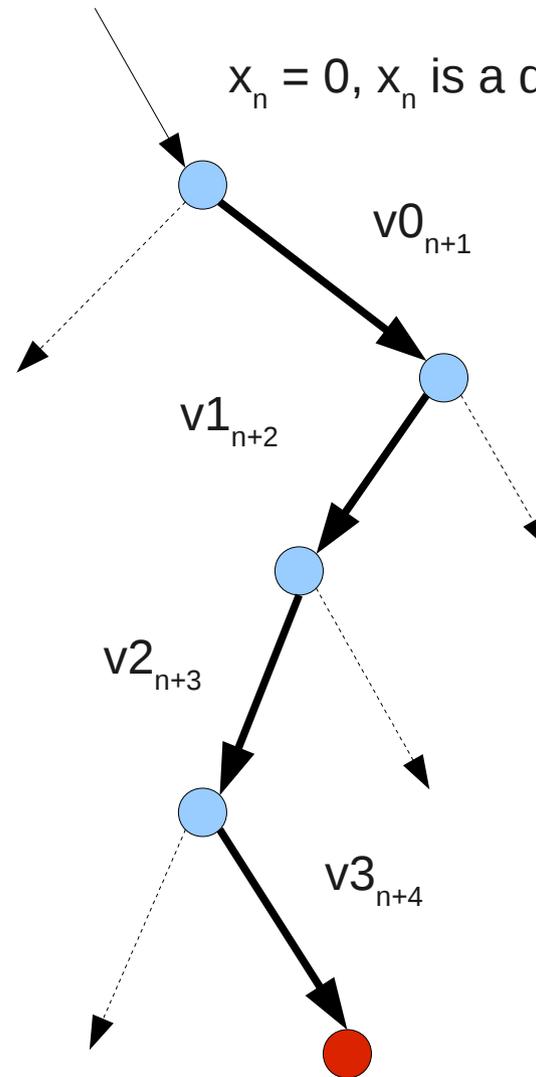


$x_n = 0$, x_n is a decision variable



DPLL ALGORITHM (CONT)

Clause Learning

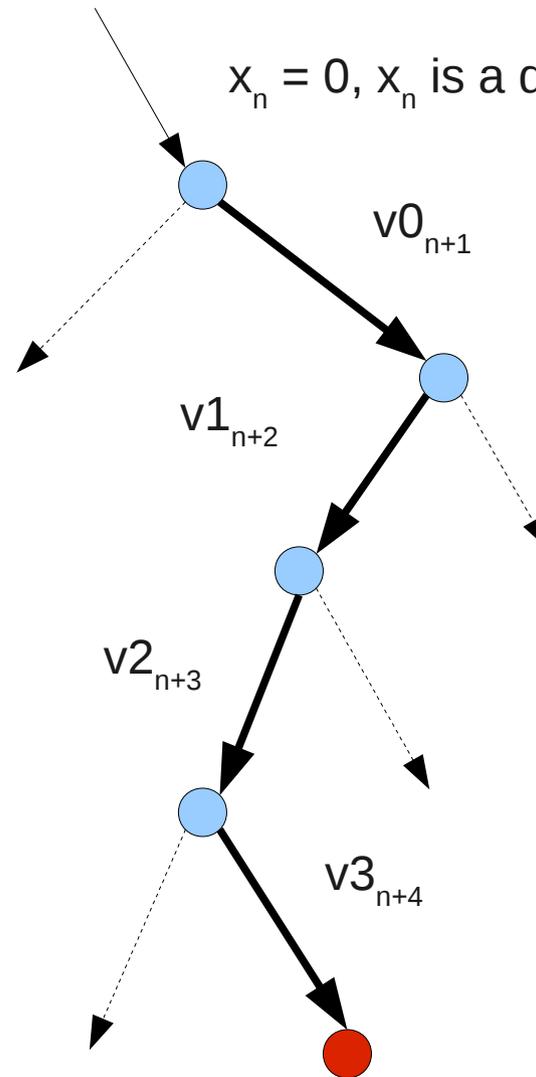


Labeled vertices are inferred by the assignment $x_n = 0$

DPLL ALGORITHM (CONT)

The learned clause is (x)

Clause Learning



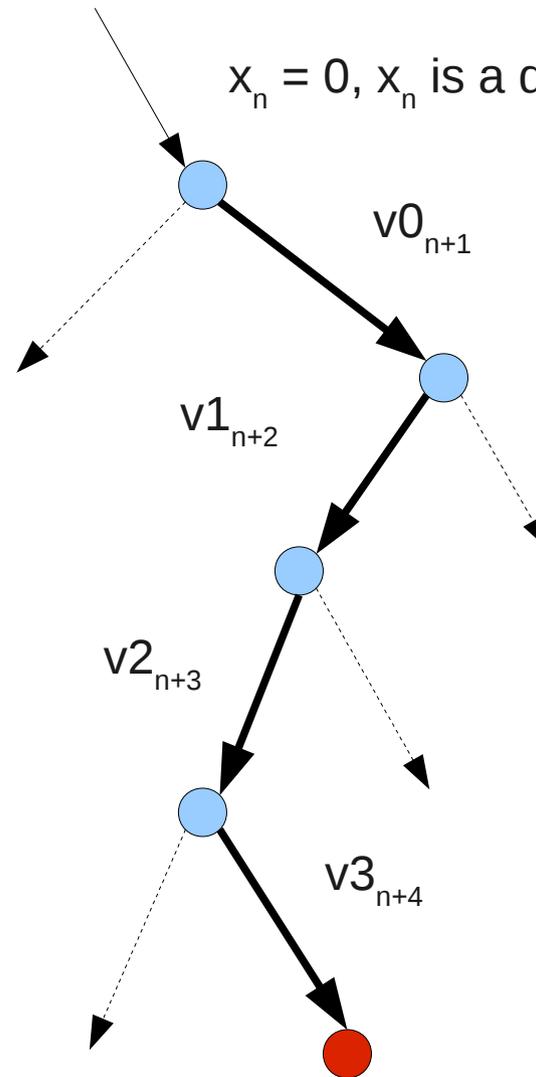
Labeled vertices are inferred by the assignment $x_n = 0$

DPLL ALGORITHM (CONT)

The learned clause is (x)

This entire sub-tree is effectively pruned

Clause Learning



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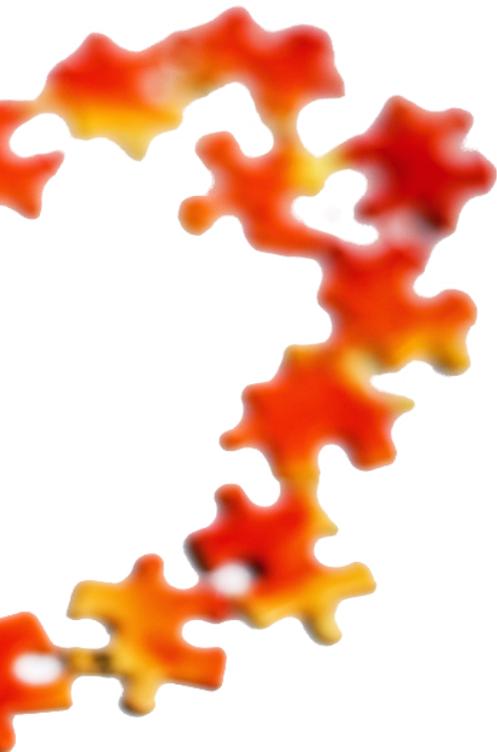
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Branch selection heuristics – Selecting the variable to assign



DPLL ALGORITHM (CONT)^[1]

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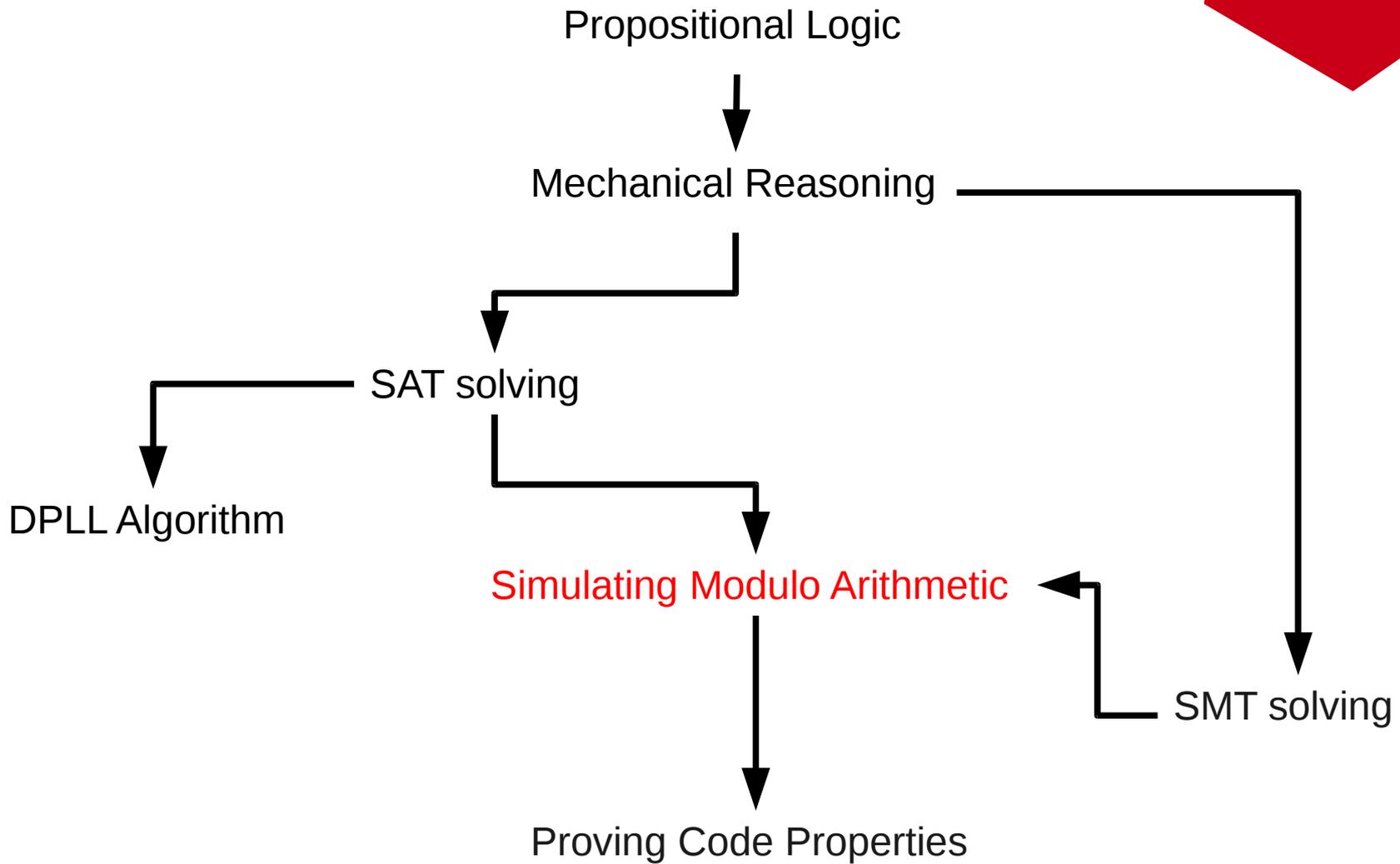
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Restarts after a given timeout to reduce sensitivity to unfortunate branch selection

[1] See Leonardo De Moura's MSR page for an excellent collection of papers on building real world solvers

PART I: DOWN THE RABBIT HOLE



MODULO ARITHMETIC & SAT

We can encode $+$, $-$, $*$, $/$, \gg , \ll
etc as operations over *bit-*
vectors



MODULO ARITHMETIC & SAT

We can encode +, -, *, /, >>, <<
etc as operations over *bit-*
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1 byte, 8 bits, 8 propositional
variables $\langle p_7 p_6 p_5 p_4 p_3 p_2 p_1 p_0 \rangle$



MODULO ARITHMETIC & SAT

We can encode +, -, *, /, >>, <<
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Encoding of a full adder
(where X is XOR)

1 byte, 8 bits, 8 propositional
variables $\langle p_7 p_6 p_5 p_4 p_3 p_2 p_1 p_0 \rangle$

$cin_n = 0$ if $n == 0$ or $carry_{n-1}$ otherwise

$sum(a_n, b_n, cin) = ((a_n X b_n) X cin_n)$

$carry(a_n, b_n, cin_n) = ((a_n \wedge b_n) \vee ((a_n X b_n) \wedge cin_n))$

MODULO ARITHMETIC & SAT

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vectors

Encoding of a full adder
(where X is XOR)

1 byte, 8 bits, 8 propositional
variables $\langle p_7 p_6 p_5 p_4 p_3 p_2 p_1 p_0 \rangle$

$cin_n = 0$ if $n == 0$ or $carry_{n-1}$ otherwise

$sum(a_n, b_n, cin) = ((a_n X b_n) X cin_n)$

$carry(a_n, b_n, cin_n) = ((a_n \wedge b_n) \vee ((a_n X b_n) \wedge cin_n))$

Can be extended to bitvectors of arbitrary
lengths and used to represent subtraction

MODULO ARITHMETIC & SAT

Why do we care about DPLL
and optimising our search?



MODULO ARITHMETIC & SAT

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Single multiplier – 8 bits^[1]

n	# Vars	# Clauses
8	313	1001
16	1265	4177
24	2857	9529
32	5089	17057
64	20417	68929

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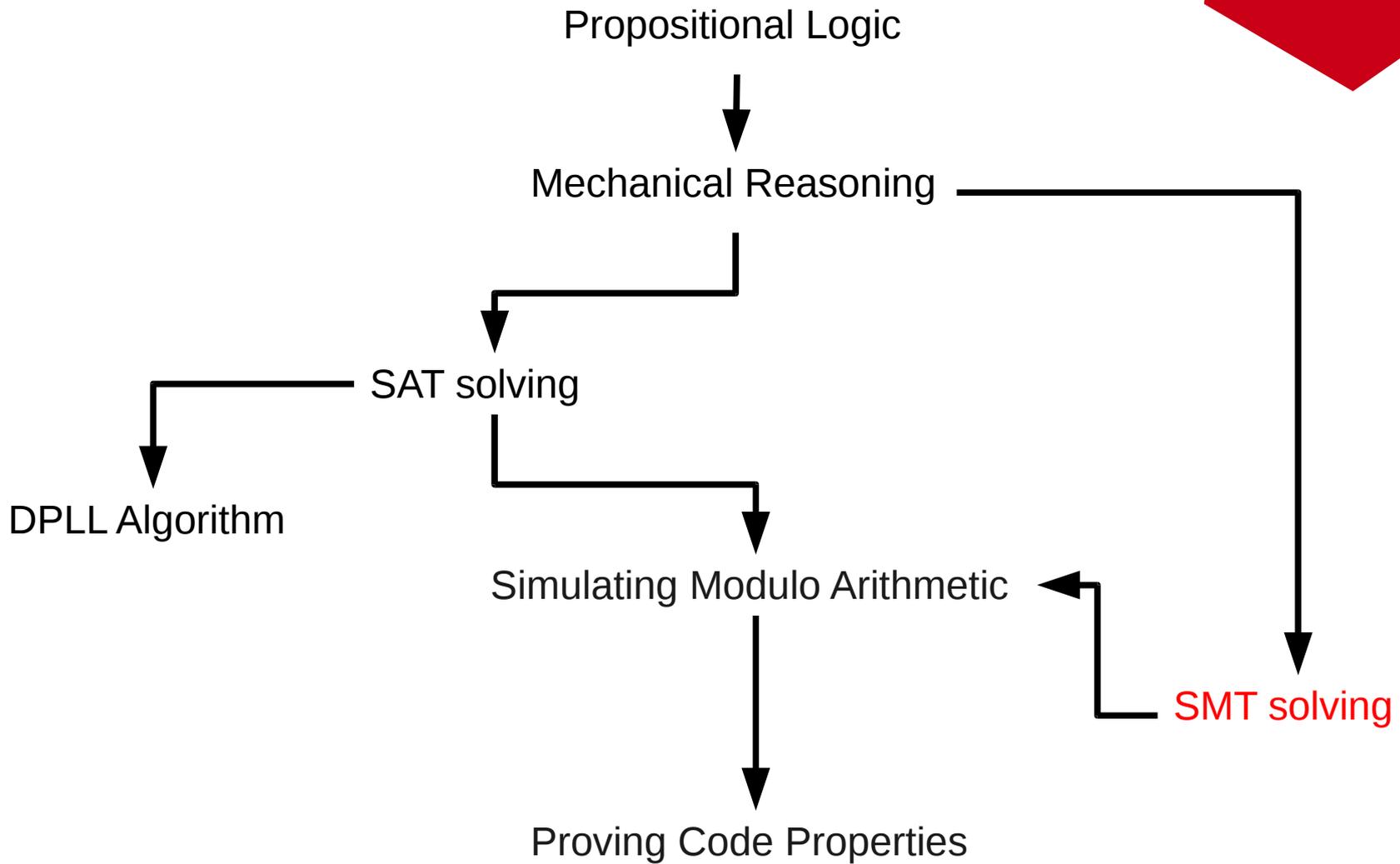
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↓
SMT solvers

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PART I: DOWN THE RABBIT HOLE



SMT SOLVERS

There are many algorithms for handling equality logic, linear/non-linear arithmetic and so forth^[1] that don't rely on flattening out the equations to bit-vector operations e.g. simplex over linear inequalities

[1] For sanity I've avoided a discussion of first order logic, decidability and combining theories that is relatively important. See Wikipedia or <http://unprotectedhex.com/psv>

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Use a theory specific solver to check if this assignment is feasible

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SMT SOLVERS

Provide a much more intuitive encoding of programming language semantics



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Theories for arrays, lists, sets etc



SMT SOLVERS

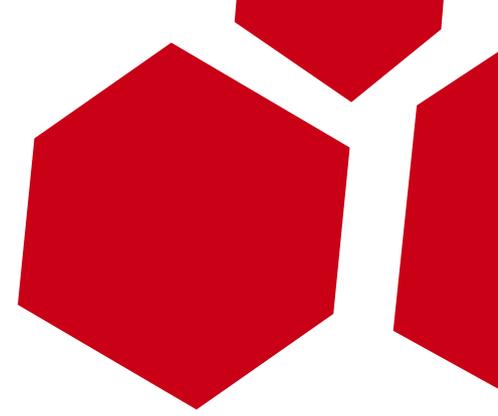
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SMT-LIB specification describes a number of base theories and provides functions over them

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SMT SOLVERS



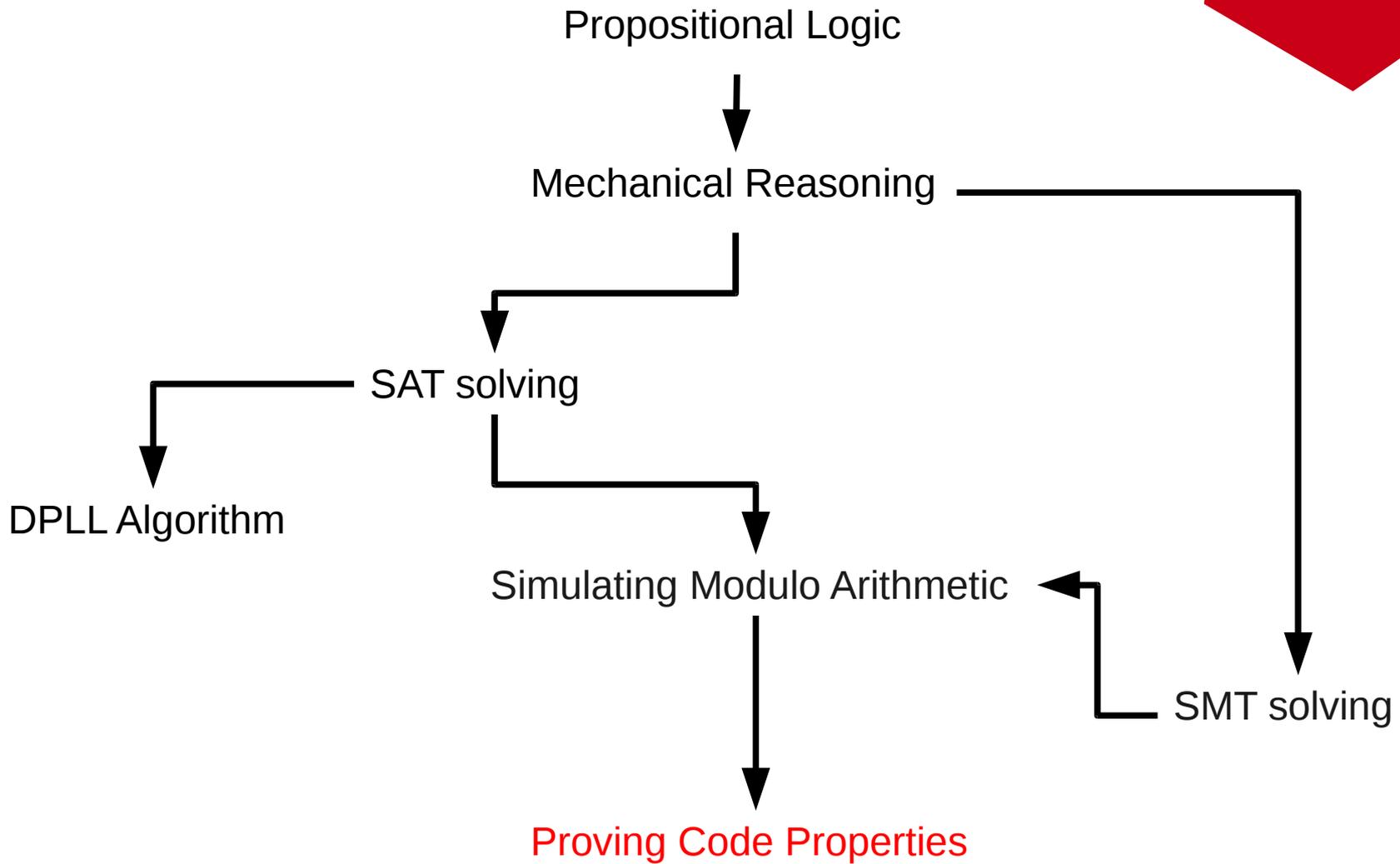
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Theories for arrays, lists, sets etc

`bvadd`, `bvmul`, `bvand`, `bvor`, `bvult`, `bvugt` etc

PART I: DOWN THE RABBIT HOLE



WebKit Code

```
void* ArrayBuffer::tryAllocate(unsigned numElements,
                               unsigned elementByteSize)
{
    void* result;
    // Do not allow 32-bit overflow of the total size
    if (numElements) {
        unsigned totalSize = numElements * elementByteSize;
        if (totalSize / numElements != elementByteSize)
            return 0;
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SMT-LIB model

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(benchmark uint_ovf
:status unknown
:logic QF_BV

:extrafuns ((totalSize BitVec[32])(numElements BitVec[32])
            (elSize BitVec[32]))

; elSize != 0
; This assumption isn't actually accounted for in the code
:assumption (bvugt elSize bv0[32])
; if (numElements) {
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; unsigned totalSize = numElements * elementByteSize;
:assumption (= totalSize (bvmul numElements elSize))

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:assumption (= elSize (bvudiv totalSize numElements))

; Our requirement totalSize < numElements
:formula (bvult totalSize numElements)
)
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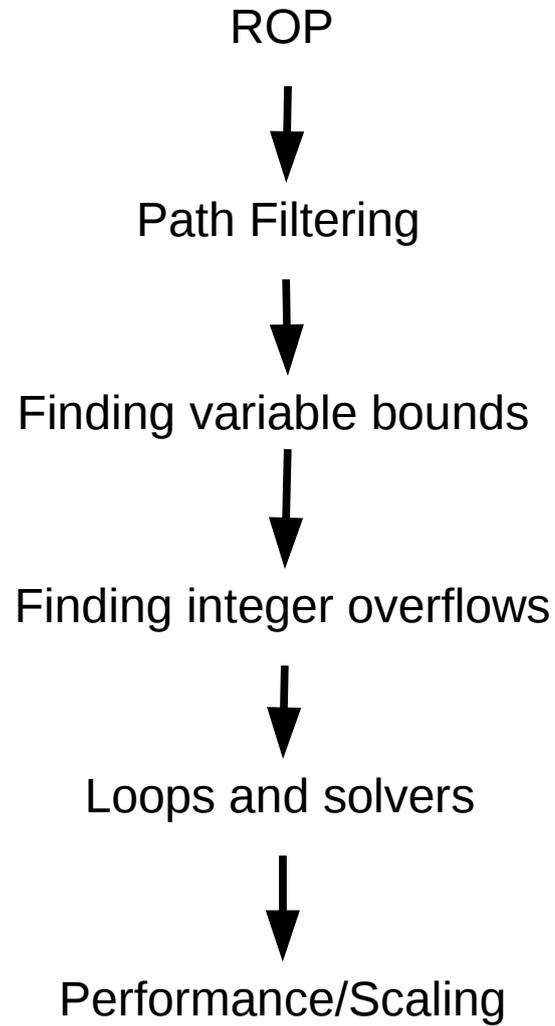
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:formula (bvult totalSize numElements)
)
```

```
[sean@sean-laptop bin]$ time ./yices -f webkit.smt
unsat
```

```
real    0m0.220s
user    0m0.212s
sys     0m0.005s
```

PART II: ONE HAMMER, MANY NAILS



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ROP



Path Filtering



Finding variable bounds



Finding integer overflows



Loops and solvers



Performance/Scaling



WHICH OF THESE EXPRESS EAX = 0

```
MOV EAX,DWORD PTR SS:[EBP-4]
POP EDI
POP ESI
POP EBX
LEAVE
RETN 4
```

```
MOV EAX,ESI
POP ESI
POP EBP
RETN 8
```

```
ADC BYTE PTR DS:[ECX+C5E82404],CL
OR AL,BYTE PTR DS:[EAX]
ADD BYTE PTR DS:[EBX+658D14EC],AL
CLC
POP EBX
POP ESI
POP EBP
RETN 10
```

```
XOR EDI,EDI
MOV EAX,EDI
POP EDI
LEAVE
RETN 4
```

```
XOR EAX,EAX
INC EAX
POP EDI
POP ESI
POP EBX
LEAVE
RETN 8
```

```
XOR EAX,EAX
POP ESI
LEAVE
RETN 4
```

```
MOV ESI,DWORD PTR SS:[EBP-8]
MOV EDI,DWORD PTR SS:[EBP-4]
SUB ESP,4
MOV ESP,EBP
POP EBP
RETN 10
```

```
SBB EAX,EAX
AND EAX,7FF6FD00
ADD EAX,80090300
POP EBP
RETN 8
```

```
ADD EAX,90302B8
ADD BYTE PTR SS:[EBP+8B0B7CC0],40
ADC AL,8B
PUSH EBP
CLD
MOV DWORD PTR DS:[ECX+4],EDX
MOV DWORD PTR DS:[ECX],ESI
POP ESI
LEAVE
RETN 10
```

```
MOV AL,BYTE PTR SS:[EBP+8]
POP EDI
POP ESI
POP EBX
LEAVE
RETN 14
```



REASONING ABOUT X86 USING SMT SOLVERS

- 1) Convert x86 to SMT representation F
(We've seen it's possible to model code as formulae so we just need to automate that)



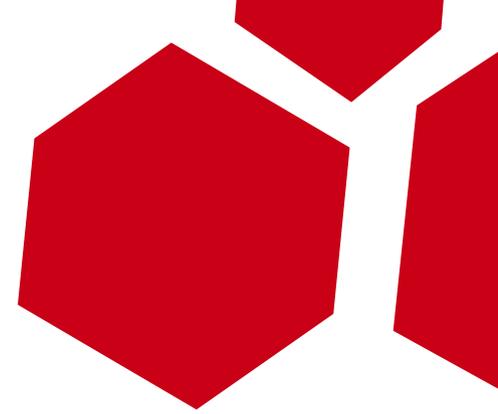
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Equivalence vs Implication
(Side effects)

EAX == 0



```
XOR EDI,EDI  
MOV EAX,EDI  
POP EDI  
LEAVE  
RETN 4
```

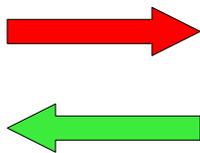


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Validity versus Satisfiability
(Context sensitive gadgets)

VS

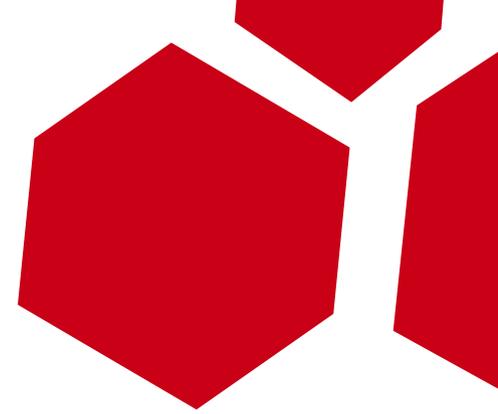
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LEAVE  
RETN 8
```



```
def analyzeXOR(self, op):  
    dst = self.buildState(op.operand[0]);  
    src = self.buildState(op.operand[1]);  
    (res,dstval,srcval)=self.solveArithmetic(self.state.solver.xorExpr,dst,src)  
    self.updateFlags("LOGIC", res, dstval, srcval)  
  
def analyzeINC(self, op):  
    cf = self.state.flags['_CF']  
    op.operand = (op.operand[0], op.constantOperand(1), op.emptyOperand())  
    self.analyzeADD(op)  
    self.state.flags['_CF'] = cf  
  
def analyzeRETN(self, op):  
    self.state.EIP = self.getMemoryStateFromSolverState(self.state.regs['ESP'], 32)  
    self.state.RETNoffset = self.state.solver.constExpr(op.op1Constant())  
    self.state.regs['ESP'] = self.state.solver.addExpr(self.state.regs['ESP'],  
                                                       self.state.solver.addExpr(  
                                                           self.state.solver.constExpr(4),  
                                                           self.state.RETNoffset))
```



REASONING ABOUT X86 USING SMT SOLVERS

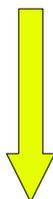
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def analyzeINC(self, op):
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    self.analyzeADD(op)
    self.state.flags['_CF'] = cf
```

```
def analyzeRETN(self, op):
    self.state.EIP = self.getMemoryStateFromSolverState(self.state.regs['ESP'], 32)
    self.state.RETNoffset = self.state.solver.constExpr(op.op1Constant())
    self.state.regs['ESP'] = self.state.solver.addExpr(self.state.regs['ESP'],
        self.state.solver.addExpr(
            self.state.solver.constExpr(4),
            self.state.RETNoffset))
```



```
def xorExpr(self, exp1, exp2):
    return self.CVC.vc_bvXorExpr(self.vc, exp1, exp2) | self.get_error()

def negExpr(self, exp):
    return self.CVC.vc_bvUminusExpr(self.vc, exp) | self.get_error()

def addExpr(self, exp1, exp2, bits=None):
    if not bits: bits=self.getBitSizeFromExpr(exp1)
    return self.CVC.vc_bvPlusExpr(self.vc, bits, exp1, exp2) | self.get_error()

def subExpr(self, exp1, exp2, bits=None):
    if not bits: bits=self.getBitSizeFromExpr(exp1)
    return self.CVC.vc_bvMinusExpr(self.vc, bits, exp1, exp2) | self.get_error()
```

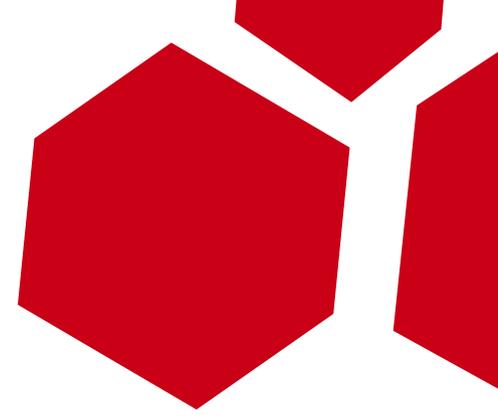


FIND_GADGET.PY # FINDING GADGETS WITH SPECIFIC SEMANTICS

Get candidate gadgets



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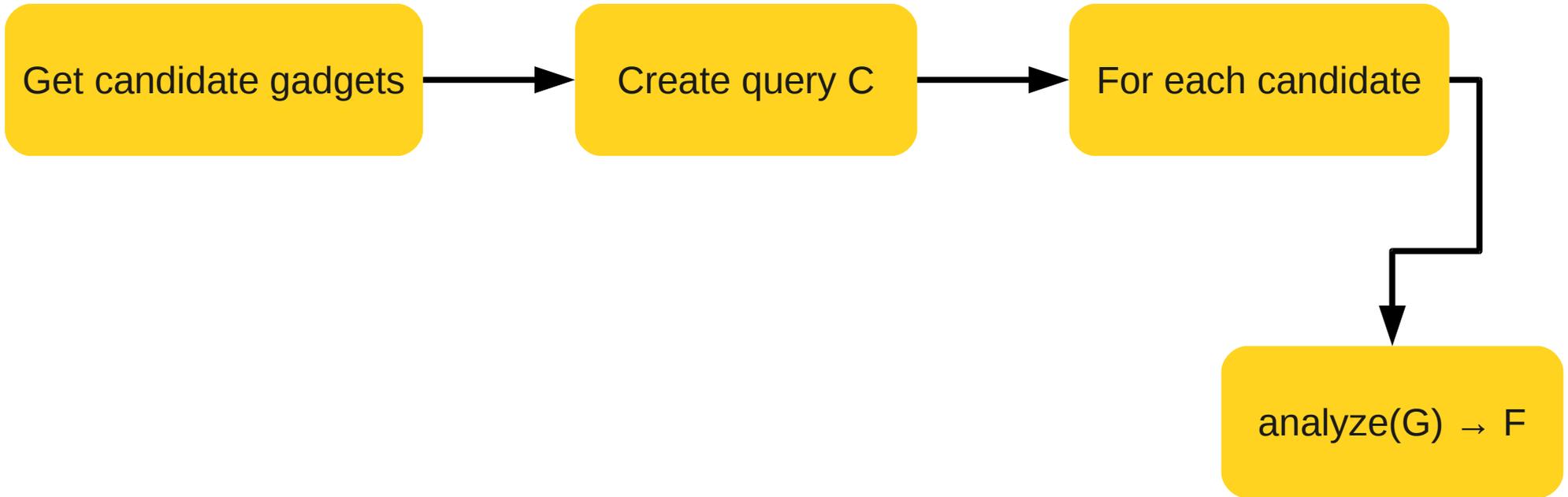


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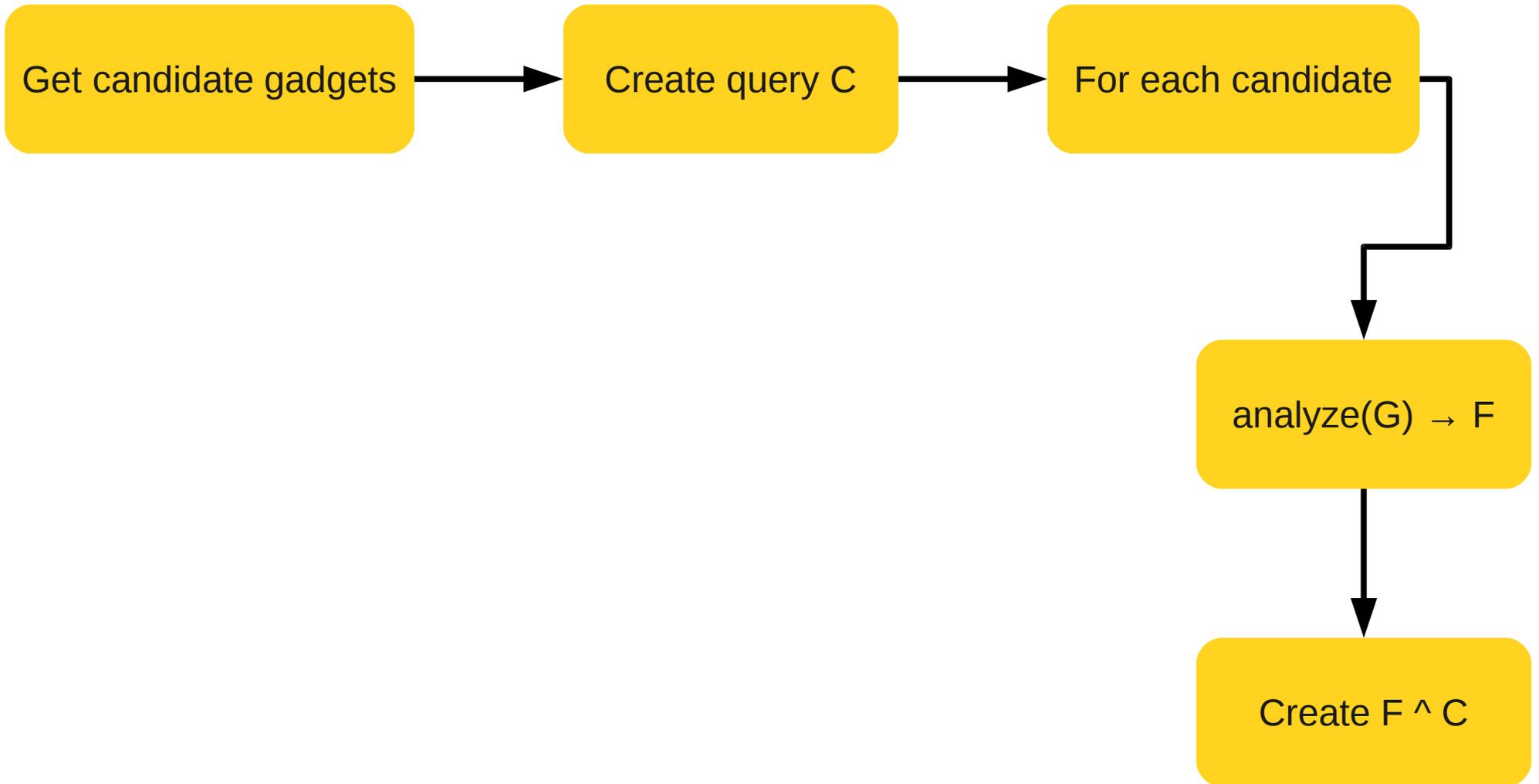


Create query C

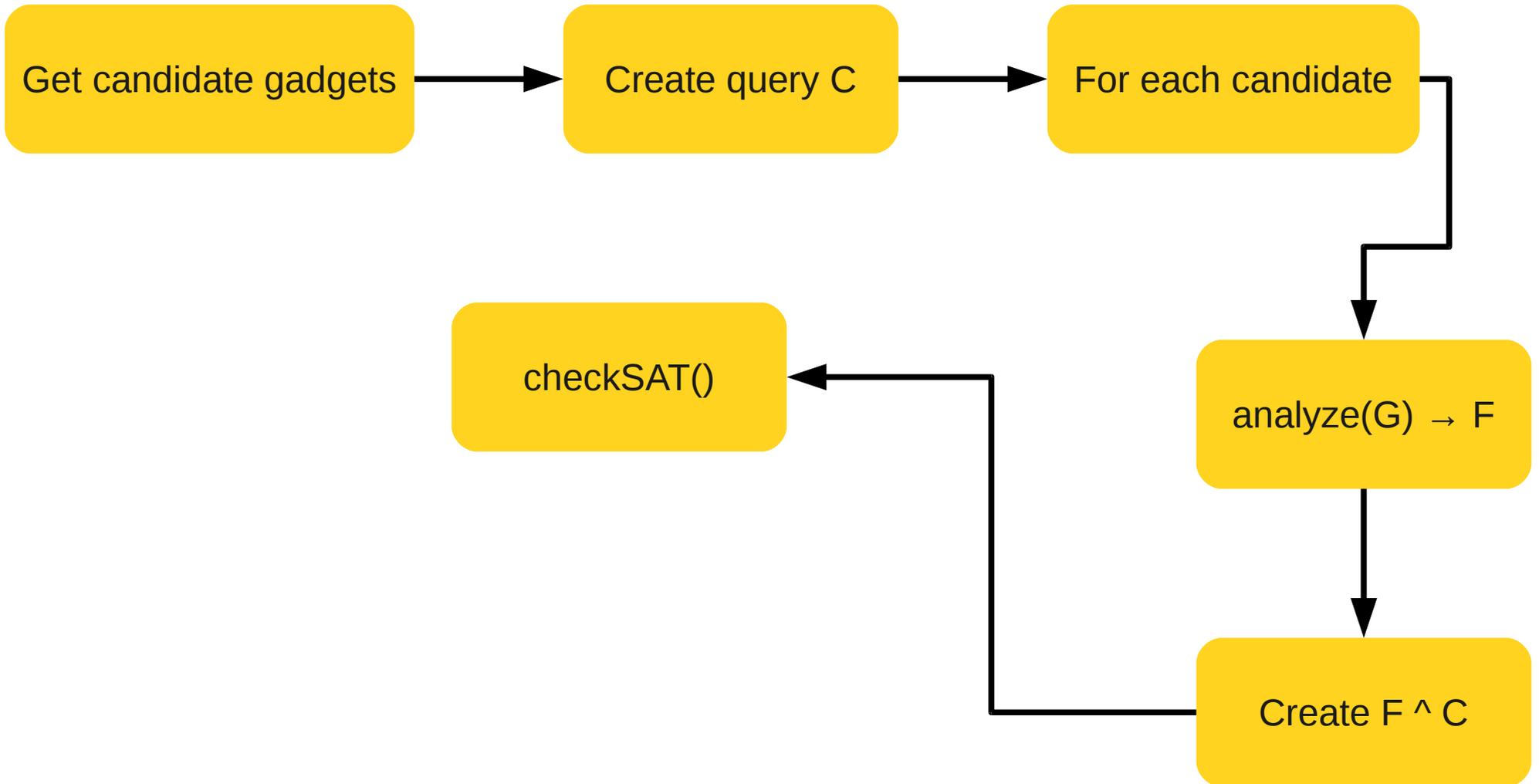
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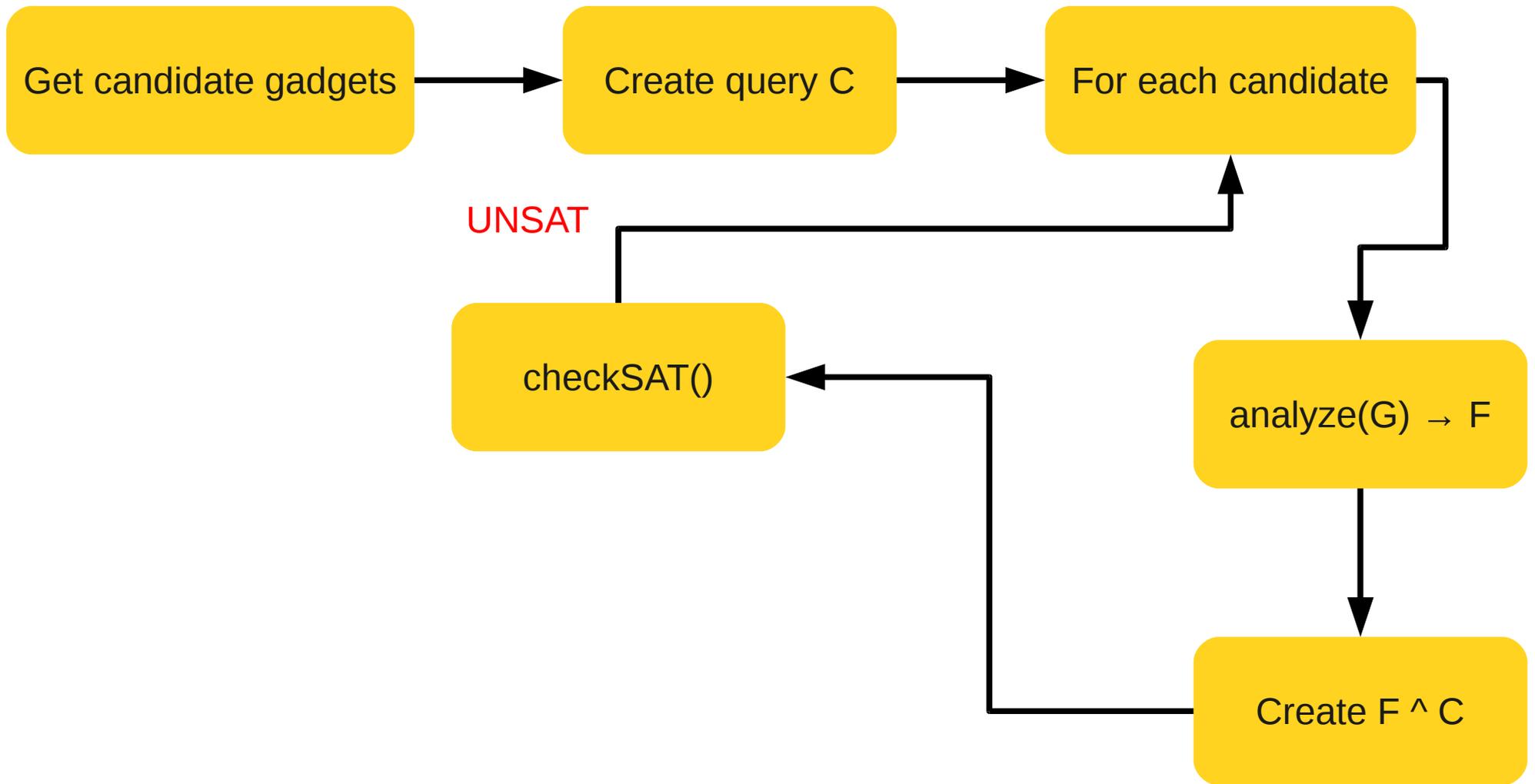
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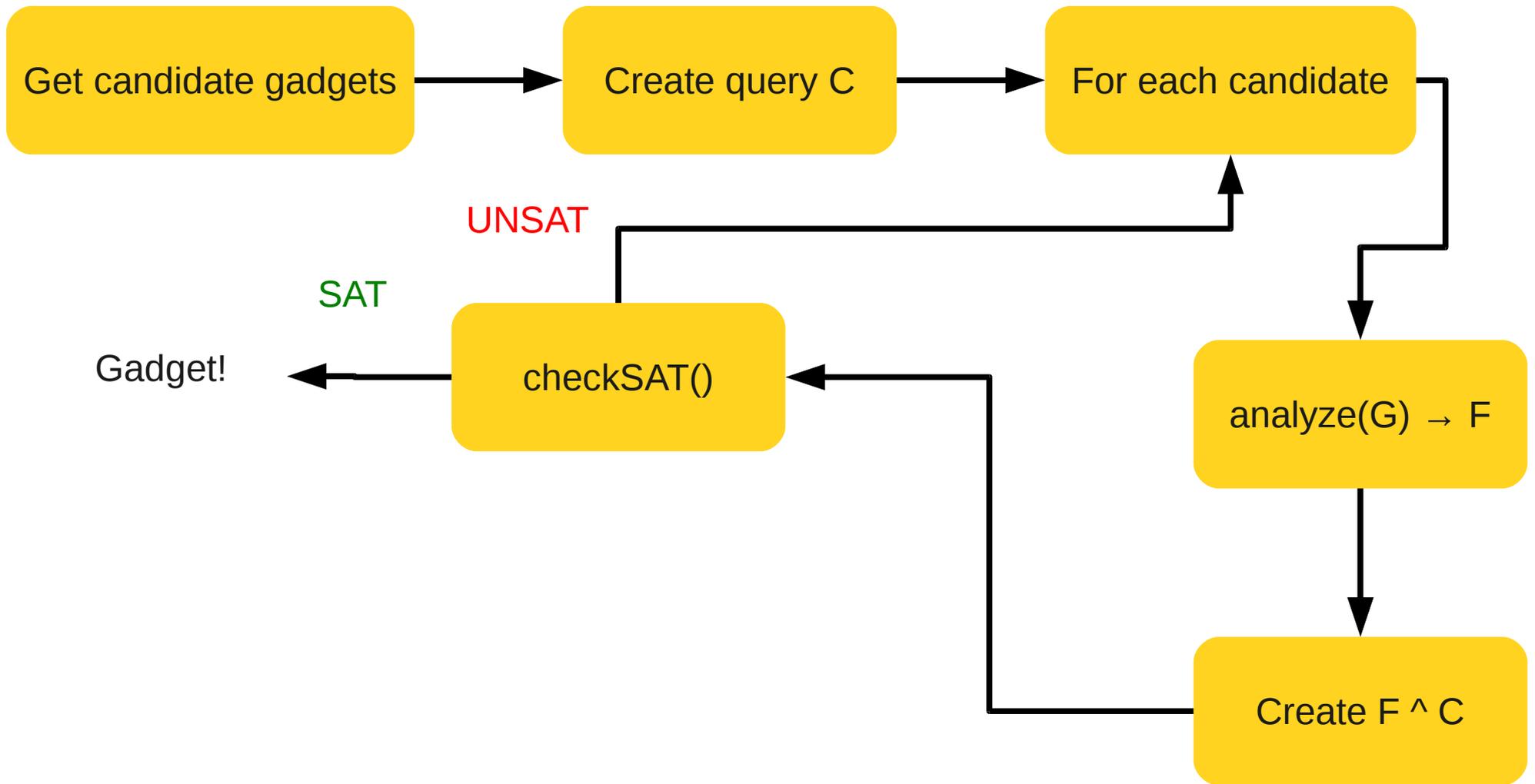
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DEMO



INFRASTRUCTURE

SequenceAnalyzer – Models x86 as operations over a set of SMT primitives

Solver – Ctypes interface to the CVC3 SMT solver API. Supports a variety of theories including quantifier free, bit-vector arithmetic, linear arithmetic etc.



PART II: ONE HAMMER, MANY NAILS



ROP



Path Filtering



Finding variable bounds



Finding integer overflows

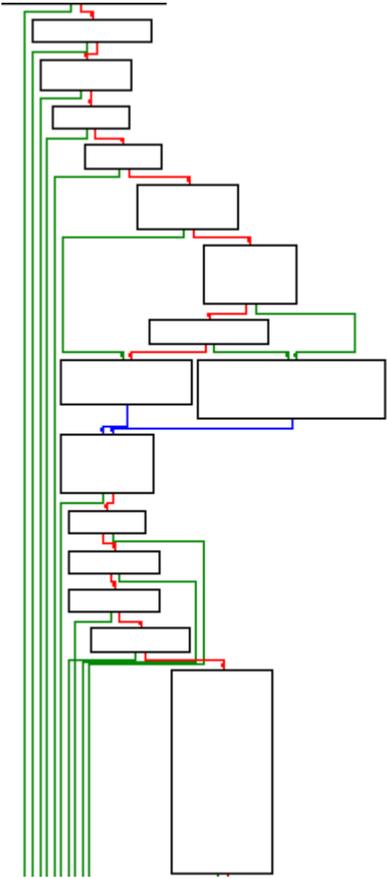


Loops and solvers



Performance/Scaling

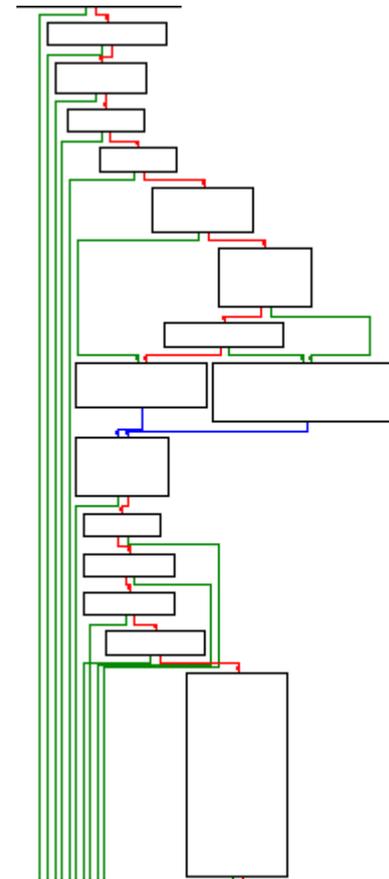
PATHOGEN.PY # FILTERING INVALID PATHS



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A problem for both manual analysis and automated tools

What paths in the CFG are actually possible given the constraints? Given a certain configuration of registers/memory?

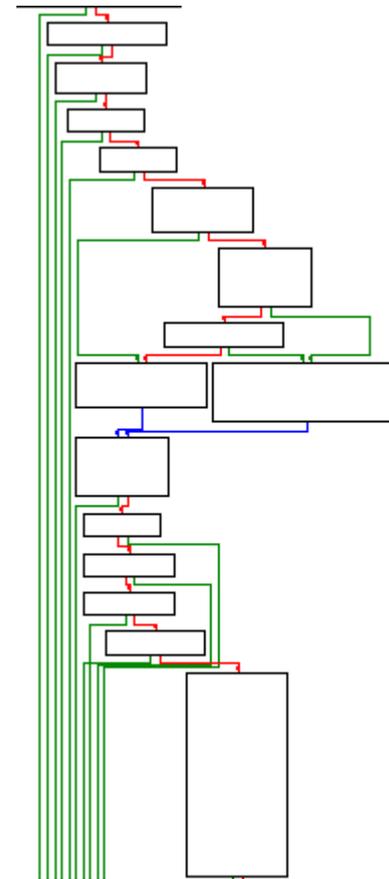


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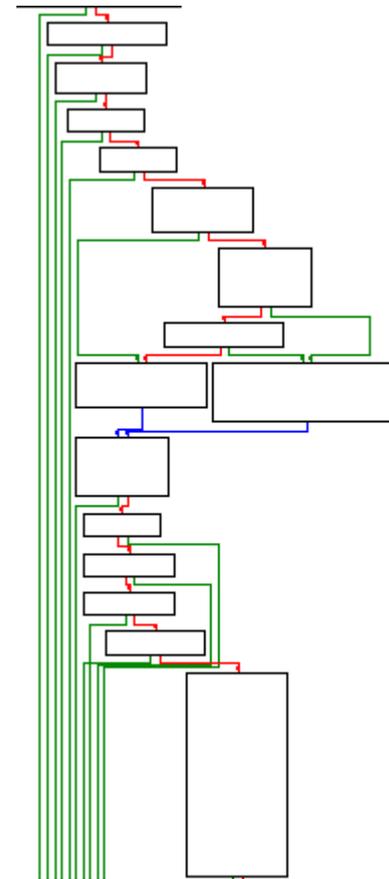
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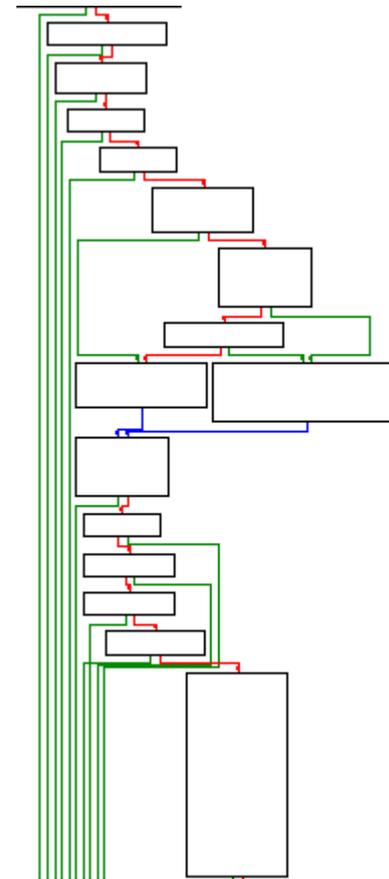
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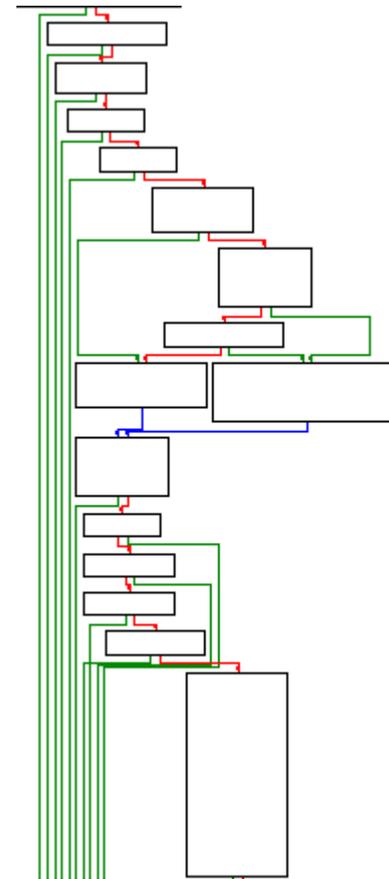
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- 1) Generate a path, `codegraph.py` + `pathgenerator.py` (No SMT involved here, just a backend for any static analysis stuff)
- 2) Build *path condition* over each path. After every conditional jmp call `checkSAT()`
- 3) Discard any paths that return UNSAT



PATHOGEN.PY # FILTERING INVALID PATHS

```
# Use the path generator to dump all possible paths
pg = PathGenerator(bb_graph.basic_blocks, bb_graph.bb_out_edges)
pg.imm = imm

cnt = 0
feasible_paths = []
for path in pg.generate_paths(start_addr):
    cnt += 1

    path.log(imm)
    if not prune_paths:
        continue

    p_walker = PathWalker(imm, debug=True)
    try:
        p_walker.walk(path)
        feasible_paths.append(path)
    except UnsatPathConditionException, e:
        imm.log("%s" % str(e))
```

Path iterator



Checks
conditions as
it walks the
path



PATHOGEN.PY # FILTERING INVALID PATHS



Check path
taken
condition



```
def analyzeJccNoFollow(self, condition, finaladdress):  
    if self.check_jcc_taken:  
        self.state.solver.push()  
        # Check if the jcc can be taken  
        ret = self.state.solver.checkUnsat(condition)  
        self.state.solver.pop()  
  
        if not ret:  
            self.jcc_taken = True  
        else:  
            self.jcc_taken = False  
        # assert the condition as true and set everything for analysis  
        self.jcc_taken_condition = condition
```

Check path
not taken
condition



```
if self.check_jcc_not_taken:  
    self.state.solver.push()  
    # Check if the fall-through is possible  
    not_cond = self.state.solver.boolNotExpr(condition)  
    ret = self.state.solver.checkUnsat(not_cond)  
    self.state.solver.pop()  
  
    if not ret:  
        self.jcc_not_taken = True  
    else:  
        self.jcc_not_taken = False  
  
    self.jcc_not_taken_condition = not_cond
```

PATHOGEN.PY # FILTERING INVALID PATHS

DEMO



INFRASTRUCTURE

SequenceAnalyzer – Models x86 as operations over a set of SMT primitives.

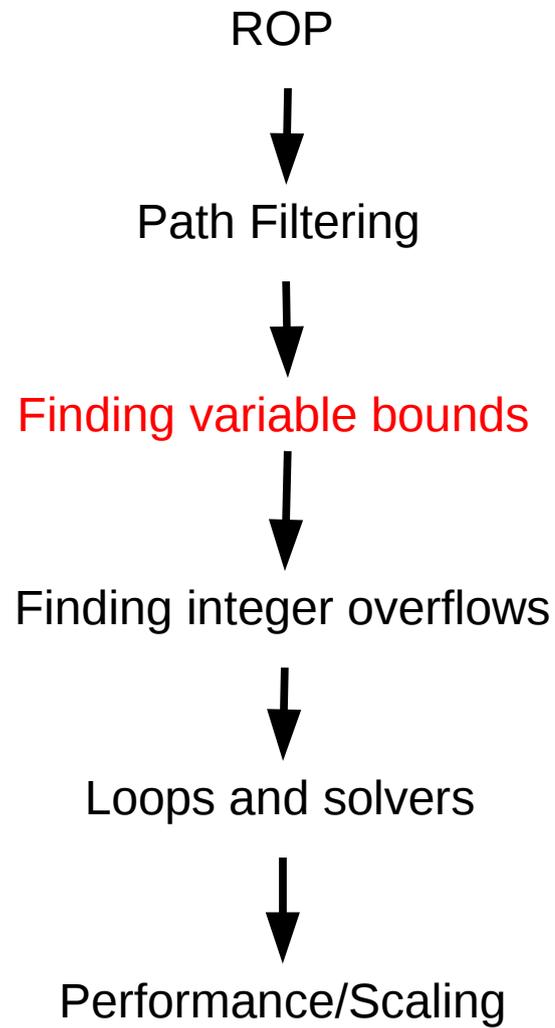
Solver – Ctypes interface to the CVC3 SMT solver API. Supports a variety of theories including quantifier free, bit-vector arithmetic, linear arithmetic etc.

CodeGraph/PathGenerator – Purely static CFG building and path generation.

PathWalker – SMT based path traversal. Each conditional jump is checked for feasibility and the path discarded if not SAT.



PART II: ONE HAMMER, MANY NAILS



VARBOUNDS.PY # FINDING VARIABLE RANGES

```
MOV ESI,EDX
SHR ESI,4
XOR ESI,ECX
AND ESI,0F0F0F0F
XOR ECX,ESI
SHL ESI,4
XOR EDX,ESI
PUSH EDI
MOV ESI,ECX
SHL ESI,12
XOR ESI,ECX
AND ESI,CCCC0000
MOV EDI,ESI
SHR EDI,12
XOR EDI,ESI
XOR ECX,EDI
MOV ESI,EDX
SHL ESI,12
XOR ESI,EDX
AND ESI,CCCC0000
MOV EDI,ESI
SHR EDI,12
XOR EDI,ESI
XOR EDX,EDI
MOV ESI,EDX
SHR ESI,1
XOR ESI,ECX
AND ESI,55555555
XOR ECX,ESI
ADD ESI,ESI
XOR EDX,ESI
MOV ESI,ECX
SHR ESI,8
XOR ESI,EDX
AND ESI,0FF00FF
XOR EDX,ESI
SHL ESI,8
XOR ECX,ESI
MOV ESI,EDX
SHR ESI,1
XOR ESI,ECX
MOV EAX,DWORD PTR SS:[EBP-
AND ESI,55555555
XOR ECX,ESI
ADD ESI,ESI
XOR EDX,ESI
MOV EDI,EDX
SHR EDI,0C
AND EDI,0FF0
MOV ESI,ECX
AND ESI,F000000F
OR EDI,ESI
MOV ESI,EDX
AND ESI,0FF
SHR EDI,4
SHL ESI,10
OR EDI,ESI
AND EDX,0FF00
OR EDI,EDX
AND ECX,0FFFFFFF
XOR EDX,EDX
MOV DWORD PTR SS:[EBP-8],E
MOV BL,BYTE PTR DS:[EDX+76
TEST BL,BL
MOV EDX,EDI
MOV ESI,ECX
```

VARBOUNDS.PY # FINDING VARIABLE RANGES

Given we control EDX at the start what range of values may ESI have at the end?

```
MOV ESI,EDX
SHR ESI,4
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XOR ECX,ESI
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XOR ECX,EDI
MOV ESI,EDX
SHL ESI,12
XOR ESI,EDX
AND ESI,CCCC0000
MOV EDI,ESI
SHR EDI,12
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XOR EDX,EDI
MOV ESI,EDX
SHR ESI,1
XOR ESI,ECX
AND ESI,55555555
XOR ECX,ESI
ADD ESI,ESI
XOR EDX,ESI
MOV ESI,ECX
SHR ESI,8
XOR ESI,EDX
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OR EDI,ESI
MOV ESI,EDX
AND ESI,0FF
SHR EDI,4
SHL ESI,10
OR EDI,ESI
AND EDX,0FF00
OR EDI,EDX
AND ECX,0FFFFFFF
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MOV DWORD PTR SS:[EBP-8],E
MOV BL,BYTE PTR DS:[EDX+76
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MOV EDI,ESI
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XOR EDI,ESI
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SHL ESI,12
XOR ESI,EDX
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ADD ESI,ESI
XOR EDX,ESI
MOV ESI,ECX
SHR ESI,8
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SHL ESI,12
XOR ESI,EDX
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XOR EDX,EDI
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SHR ESI,1
XOR ESI,ECX
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OR EDI,ESI
MOV ESI,EDX
AND ESI,0FF
SHR EDI,4
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C: $(= ebx^2, x)$ for all x in $[0, \dots, 2^n]$

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SHR EDI,12
XOR EDI,ESI
XOR EDX,EDI
MOV ESI,EDX
SHR ESI,1
XOR ESI,ECX
AND ESI,55555555
XOR ECX,ESI
ADD ESI,ESI
XOR EDX,ESI
MOV ESI,ECX
SHR ESI,8
XOR ESI,EDX
AND ESI,0FF00FF
XOR EDX,ESI
SHL ESI,8
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SHR EDI,0C
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MOV ESI,ECX
AND ESI,F000000F
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AND ESI,0FF
SHR EDI,4
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MOV EDX,EDI
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Every SAT result indicates that x is a possible output value and `getConcreteModel()` gives the value required in EDX to achieve it

```
MOV ESI,EDX
SHR ESI,4
XOR ESI,ECX
AND ESI,0F0F0F0F
XOR ECX,ESI
SHL ESI,4
XOR EDX,ESI
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MOV ESI,ECX
SHR ESI,8
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XOR EDX,ESI
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XOR ECX,ESI
MOV ESI,EDX
SHR ESI,1
XOR ESI,ECX
MOV EAX,DWORD PTR SS:[EBP-
AND ESI,55555555
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SHR EDI,0C
AND EDI,0FF0
MOV ESI,ECX
AND ESI,F000000F
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MOV DWORD PTR SS:[EBP-8],E
MOV BL,BYTE PTR DS:[EDX+76
TEST BL,BL
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```

VARBOUNDS.PY # FINDING VARIABLE RANGES

Better solution? Use bucket ranges. Split the range $0, 2^n$ into buckets and make C $lower_bound \leq v < upper_bound$ for each bucket. Direct $==$ queries for all values in the valid buckets. Same worst case running time. Performs far better in many cases.

```
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SHR ESI,4
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XOR ECX,ESI
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SHR EDI,4
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OR EDI,ESI
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MOV DWORD PTR SS:[EBP-8],E
MOV BL,BYTE PTR DS:[EDX+76
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MOV EDX,EDI
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```

VARBOUNDS.PY # FINDING VARIABLE RANGES

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Better still? For each bit b in r check if $b == 1$ is satisfiable in order to find an absolute upper/lower bound before the previous stage. 32 queries, works well.

```
MOV ESI,EDX
SHR ESI,4
XOR ESI,ECX
AND ESI,0F0F0F0F
XOR ECX,ESI
SHL ESI,4
XOR EDX,ESI
PUSH EDI
MOV ESI,ECX
SHL ESI,12
XOR ESI,ECX
AND ESI,CCCC0000
MOV EDI,ESI
SHR EDI,12
XOR EDI,ESI
XOR ECX,EDI
MOV ESI,EDX
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XOR EDX,EDI
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SHR ESI,1
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OR EDI,ESI
MOV ESI,EDX
AND ESI,0FF
SHR EDI,4
SHL ESI,10
OR EDI,ESI
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MOV DWORD PTR SS:[EBP-8],E
MOV BL,BYTE PTR DS:[EDX+76
TEST BL,BL
MOV EDX,EDI
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```

VARBOUNDS.PY # FINDING VARIABLE RANGES

DEMO



VARBOUNDS.PY # FINDING VARIABLE RANGES

We're still being rather dumb.



VARBOUNDS.PY # FINDING VARIABLE RANGES

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```
add eax, 10
mul ebx
rol ebx, ecx
```

Pure SMT solutions tend to have difficulty seeing the forest for the trees.



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Often worth considering using an initial static analysis run first to limit cases and use a solver to resolve any remaining imprecision.

```
mov ebx, eax
add ebx, 0xFF
and ebx, 0xFF
shl ebx, 0x10
and ebx, ecx
```



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```
cmp eax, 0xFF
jbe EXIT
```

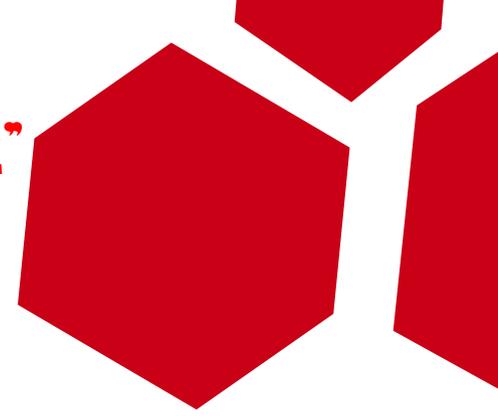
```
mov ebx, eax
add ebx, 0xFF
and ebx, 0xFF
shl ebx, 0x10
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```

Quite a lot of latent information in arithmetic, logical and conditional branching instructions that can be extracted at varying expense



ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

Abstract Interpretation is a useful framework in many situations e.g. for *varbounds.py* and logical operators



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- 2) Build an abstraction function for each concrete instruction

Three valued logic

```
{  
    MUST_BE_SET,  
    CANT_BE_SET,  
    POSSIBLY_SET  
}
```

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}
```

AND # $f(x, y)$

```
f(MBS, MBS) -> MBS  
f(MBS, CBS) -> CBS  
f(MBS, PBS) -> PBS  
f(CBS, *)    -> CBS  
f(PBS, MBS) -> PBS  
f(PBS, PBS) -> PBS  
f(PBS, CBS) -> CBS
```

ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

Abstract Interpretation is a useful framework in many situations e.g. for *varbounds.py* and logical operators

- 1) Pick an abstract domain
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Abstract Interpretation is a useful framework in many situations e.g. for *varbounds.py* and logical operators

- 1) Pick an abstract domain
- 2) Build an abstraction function for each concrete instruction
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Similar to our single bit queries but often far less computationally complex. In general makes many more problems tractable than a pure SMT based solution can't handle efficiently.

Three valued logic

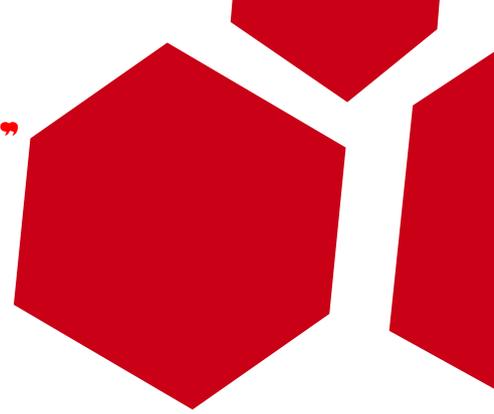
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```
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f(PBS, MBS) -> PBS  
f(PBS, PBS) -> PBS  
f(PBS, CBS) -> CBS
```

ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

Initial state: $EAX_{0-31} = \text{PBS}$,
 $ECX_{0-7} = \text{PBS}$,
 $ECX_{8-31} = \text{MBS}$

```
mov ebx, eax
add ebx, 0xFF
and ebx, 0xFF
shl ebx, 0x10
and ebx, ecx
```



ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

Initial state: $EAX_{0-31} = \text{PBS}$,
 $ECX_{0-7} = \text{PBS}$,
 $ECX_{8-31} = \text{MBS}$

```
mov ebx, eax
add ebx, 0xFF
and ebx, 0xFF
shl ebx, 0x10
and ebx, ecx
```

```
mov ebx, eax ;  $EBX_{0-31} = \text{PBS}$ 
```

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 $ECX_{0-7} = \text{PBS}$,
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```
mov ebx, eax ;  $EBX_{0-31} = \text{PBS}$ 
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```
add ebx, 0xFF ; NOP in this domain
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ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

Initial state: $EAX_{0-31} = PBS,$
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```
mov ebx, eax
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and ebx, ecx
```

```
mov ebx, eax ;  $EBX_{0-31} = PBS$ 
```

```
add ebx, 0xFF ; NOP in this domain
```

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and ebx, 0xFF ;  $EBX_{0-7} = PBS, EBX_{8-31} = CBS$ 
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```

```
add ebx, 0xFF ; NOP in this domain
```

```
and ebx, 0xFF ;  $EBX_{0-7} = \text{PBS}$ ,  $EBX_{8-31} = \text{CBS}$ 
```

```
shl ebx, 0x10 ;  $EBX_{16-23} = \text{PBS}$   
;  $EBX_{24-31, 0-15} = \text{CBS}$ 
```

ABSTRACT INTERPRETATION IN BRIEF AND VAGUE “DETAIL”

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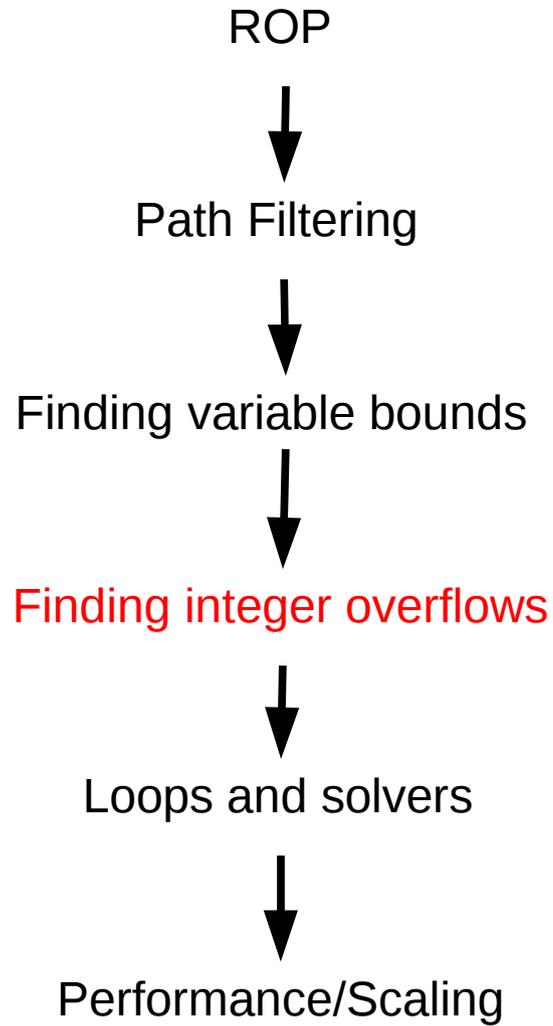
```
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```

```
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```

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```

```
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PART II: ONE HAMMER, MANY NAILS



FIND_INT_OVERFLOW.PY # WHAT IT SOUNDS LIKE

SequenceAnalyzer() takes a list of bug checkers that will be called on each instruction (although if we use it through *PathWalker()* we get path filtering as well)



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```
def check_ins(self, sa, ins):
    res = None

    op = operations.operation(ins)
    disasm_str = op.removeLockPrefix()

    if disasm_str == "ADD":
        if self.debug:
            self.imm.log("check_ins (%s): ADD" % hex(ins.getAddress()),
                        ins.getAddress())
            solver = sa.state.solver

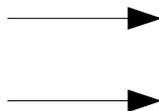
            dst = sa.buildState(ins.operand[0])
            src = sa.buildState(ins.operand[1])
            dst_val = sa.getValueFromState(dst)
            src_val = sa.getValueFromState(src)

            res_64 = solver.addExpr(dst_val, src_val, 64)

            gt_expr = solver.gtExpr(res_64, solver.constExpr(MAX_INT_32))
            status = solver.checkSat(gt_expr)

        if status:
            if self.debug:
                self.imm.log("check_ins (%s): Bug found" % \
                            hex(ins.getAddress()))
            res = BugCheckResults(ins.getAddress(),
                                  solver.getConcreteModel())
```

Represent the *ADD* in the
current context



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Represent the *ADD* in the current context



Check if the result is $> 2^{32}$



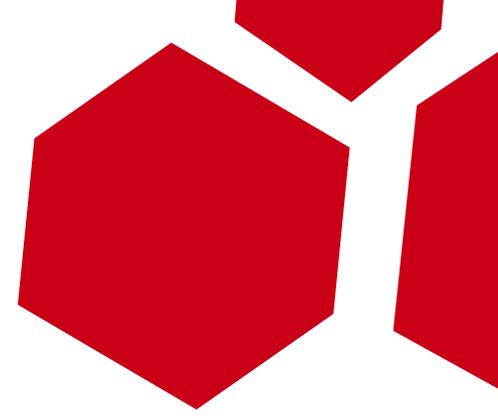
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DEMO



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Necessary to use lazy warning of bugs e.g. where the result of an overflow is used as opposed to where it occurs. Many overflows are later checked for and benign.

```
unsigned a, alloc_size;
alloc_size = get_from_user();

a = alloc_size + 1;

if (alloc_size > 0xff)
    goto exit;

x = malloc(a);
```

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```

See Julien Vanegue's HES 2009 talk for a more developed idea focusing on integer overflows on the size parameter to heap allocations

INFRASTRUCTURE

SequenceAnalyzer – Models x86 as operations over a set of SMT primitives.

Solver – Ctypes interface to the CVC3 SMT solver API. Supports a variety of theories including quantifier free, bit-vector arithmetic, linear arithmetic etc.

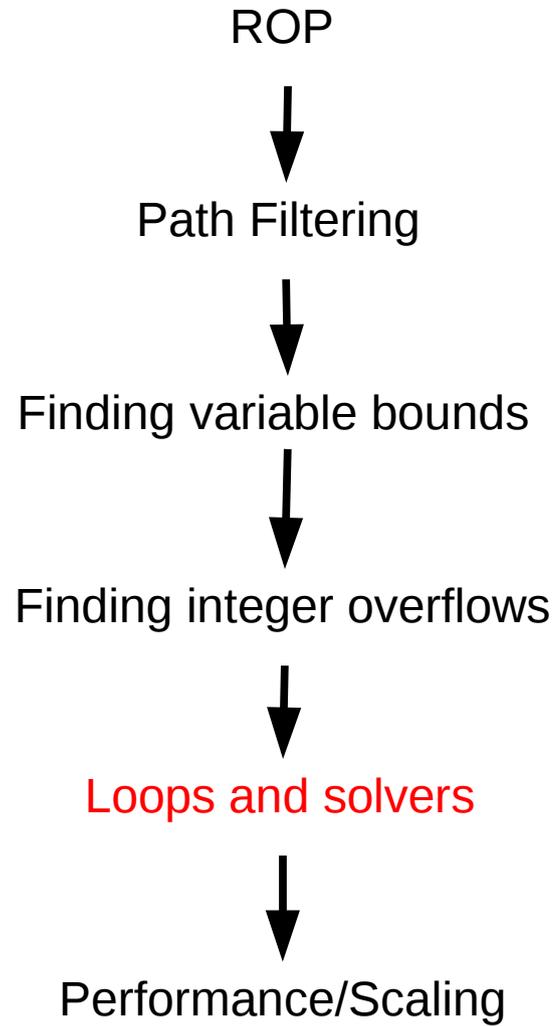
CodeGraph/PathGenerator – Purely static CFG building and path generation.

PathWalker – SMT based path traversal. Each conditional jump is checked for feasibility and the path discarded if not SAT.

BugChecker – Subclasses provide the check_ins method which will be passed the SMT context representing the current path.



PART II: ONE HAMMER, MANY NAILS



LOOPS IN THE WORLD OF SMT/SAT?

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add ebx, 0xFF =>
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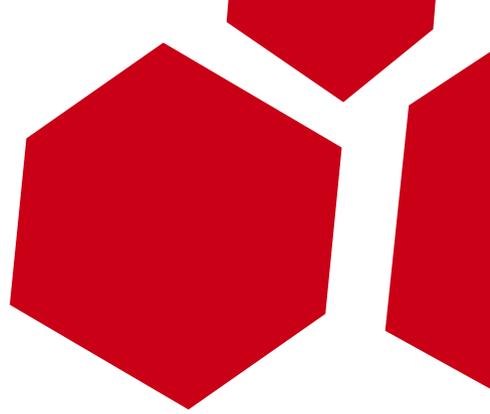


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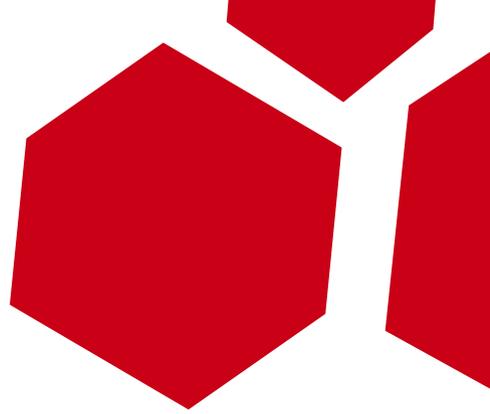
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- 1) Prove loop bounds
- 2) Guess loop bounds.



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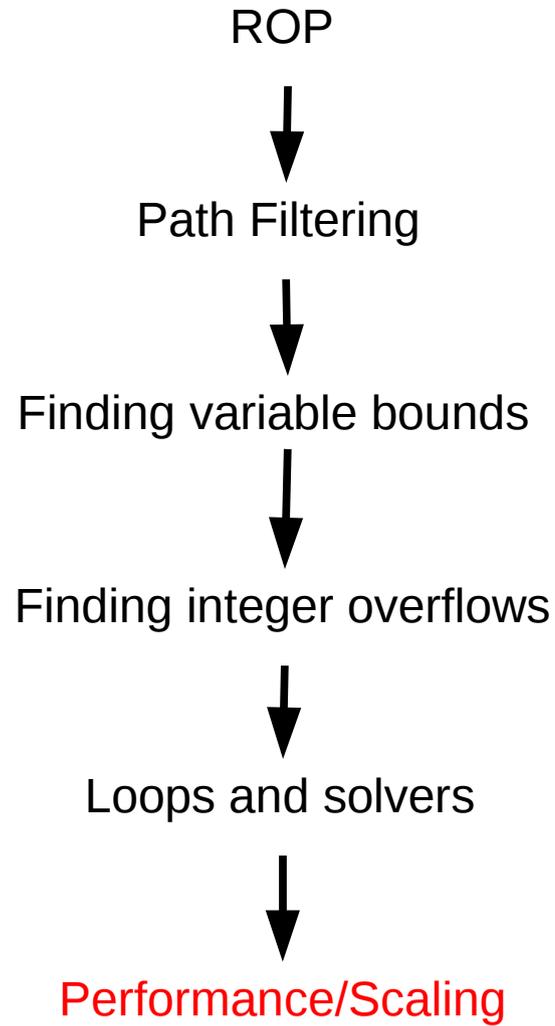
Loops however have no natural representation. Only option is to unroll. How?

- 1) Prove loop bounds
- 2) Guess loop bounds.
- 3) Approximate loop bounds



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PERFORMANCE/SCALING

Scaling of raw solver capabilities^[1]



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More investigation required to discover typical formula complexity for general RE/Exploit dev problems. SMT-COMP has no such tests.

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SMT solving tech has evolved quite a lot over the past decade to the point where it is usable as an integrated part of our exploit dev and RE processes.



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Some problems are naturally ported to this domain (path filtering) while others (variable bound checking) are more of a cludge. More still (finding arithmetic flaws) suit collaboration with basic static analysis and a human.





QUESTIONS?

SEAN HEELAN

SEAN@IMMUNITYINC.COM